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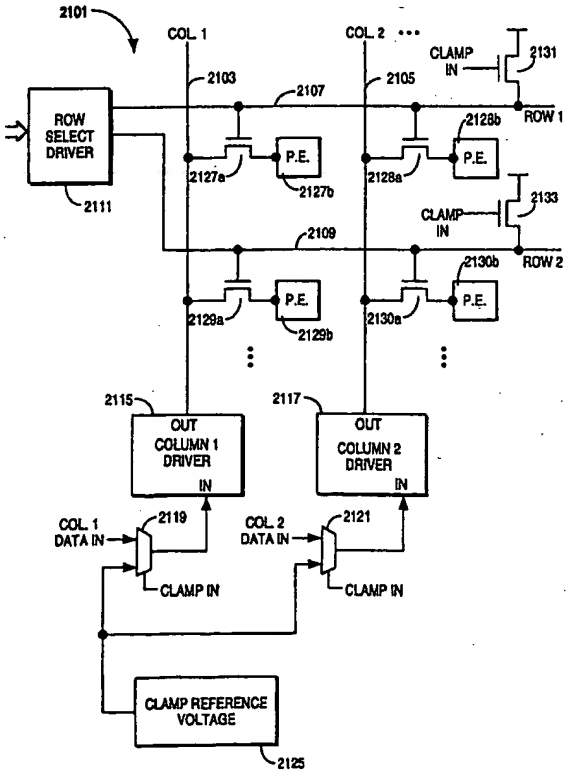
(57) Abstract

Methods and apparatuses for display systems which modulate a control electrode to cause an electro–optic layer to be reset to a state in which display data is not viewable. In one embodiment of the invention, a display system includes a first substrate having a first plurality of pixel electrodes for receiving a first plurality of pixel data values representing a first image to be displayed. The display system further includes an electro–optic layer which is operatively coupled to the pixel electrodes, a control device coupled to at least one of the pixel electrodes and an electrode operatively coupled to the electro–optic layer. The display system displays the first image and then applies a first control voltage to the electrode to alter a state of the electro–optic layer such that the first image is substantially not displayed and then the display system displays a second image represented by a second plurality of pixel data values after the electrode receives a second control voltage. The control device applies a first reference voltage to the at least one pixel electrode before the display system displays the second image. Various other apparatuses and methods are described.



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DISPLAY SYSTEM WHICH APPLIES REFERENCE VOLTAGE TO PIXEL ELECTRODES BEFORE DISPLAY OF NEW IMAGE

BACKGROUND OF THE INVENTION

The present application is a continuation-in-part of co-pending U.S. Patent Application Serial No. 08/801,994, which was filed on February 18, 1997, which is a continuation-in-part of co-pending U.S. Patent Application Serial No. 08/770,233, which was filed on December 19, 1996 by the same inventor under the title "Display System Having Common Electrode Modulation". This present application hereby claims the benefit of these earlier filing dates under 35 U.S.C. §120.

Field of the invention

The present invention relates generally to a display system, such as a liquid crystal display system. The present invention also relates to a system for providing electrical driving of an electrode of a display system. More particularly, the invention relates to a system for electrically driving an electrode of a display system to various voltages in a controlled phase relationship to the update of pixel data.

Background of the Related Art

A class of display systems operate by electrically addressing a thin, intervening layer of electro-optic material, such as liquid crystal, which is positioned between two substrates. In these display systems, it is important to achieve good display characteristics including: color purity, high contrast, high brightness, and a fast response.

High independence of frames or subframes ensures the lack of coupling between intensity values at a given pixel from one frame to the next. For example, if a pixel is to be at its brightest gray level during a first frame and then at its darkest gray level at the next frame, then a high independence would ensure that this is possible whereas a low independence would cause the pixel to appear brighter than the darkest gray level during the second frame. This coupling can cause problems such as motion smearing. High frame-to-frame independence is

important whether or not the display is a color or black-and-white (monochrome) or gray-scale display.

The level of contrast achievable is determined by the range of intensity attainable between the brightest gray level and the darkest gray level for a given pixel within a given frame or subframe.

In addition to contrast, it is desirable that the display be capable of displaying a bright image since brighter images are perceived as having a higher quality by a user.

Finally, the speed of display is determined by its ability to display one frame after the other at a high rate. If visual motion is to be displayed, flicker and other problems can be avoided only if the full color frames are displayed at a rate of at least 30 Hz and preferably 60 Hz or faster.

This speed requirement becomes even more stringent if the display does not contain a red, green, and blue pixel all at one pixel location (in other words, red, green and blue subpixels for each pixel location) but instead only has a single pixel. One type of such a display is a color sequential liquid crystal display as discussed in " Color-Sequential Crystalline-Silicon LCLV based Projector for Consumer HDTV" by Sayyah, Forber, and Efrom in SID digest (1995) pages 520-523. In those types of displays, if a display requires the sequential display of the red, green, and blue subframes, those subframes must be displayed at yet a rate higher than 90 HZ and preferable greater than 180 HZ to avoid flicker. For color sequential displays, high frame or subframe independence is required to display images with good color purity.

Any of the general display systems that operate by electrically addressing a thin, intervening layer of electro-optic material, such as liquid crystal, which is positioned between two substrates include the following characteristics. At least one of the two substrates is transparent or translucent to light and one of the substrates includes a plurality of pixel electrodes. Each pixel electrode corresponds to one pixel (or one subpixel) of the display, and each of the former may be driven independently to certain voltages so as to control the intervening electro-optic layer in such a way as to cause an image to be displayed on the electro-optic layer of the display. Sometimes each pixel can include a color triad of pixel electrodes. The second substrate of such a prior art display system has a single electrode, known as the common electrode or cover glass electrode, which

serves to provide a reference voltage so that the pixel electrodes can develop an electric field across the intervening layer of electro-optic material.

One example of such a system is a color thin film transistor (TFT) liquid crystal display. These displays are used in many notebook-sized portable computers. Colors are generated in these displays by using RGB pixel triads in which each pixel of the triad controls the amount of light passing through its corresponding red, green, or blue color filter. These color filters are one of the most costly components of a TFT display.

The major obstacle of display systems of this type is that the results of replicating the pixel electrodes, data wire, and thin film transistors, three times at each color pixel are increased cost and reduced light transmission, requiring more peripheral backlights and increased power consumption.

The other issues of high frame-to-frame independence, high contrast, and brightness become even more difficult to achieve as display rates increase.

Many approaches have been implemented to improve display characteristics of the above type displays. One common approach involves the use of a common electrode driving circuit and driving that common electrode with as flat a common electrode rectangular driving voltage as possible. By doing so, the voltage across the liquid crystal portion at that pixel is more constant, which in turn should yield improved contrast and pixel brightness.

For example, U.S. Patent 5,537,129 discloses a display system with a common electrode which attempts to achieve a flat rectangular common electrode driving voltage. Referring to Figure 2 of that patent, a common electrode 24 is connected to its driving circuit 20 through a resistor 3b. This corrects for resistive losses at 3a and capacitive coupling to the common electrode 24 from pixels and data wires. This ensures that detection device 21 with a high input impedance can be used to make a correction so the output voltage appears to be more rectangular-like. Figures 5, 9b, 11(c), and 11(d) of that U.S. patent all show the desired rectangular waveforms.

Another example of this is shown with U.S. Patent 5,561,442, which shows that with the properly applied common electrode voltage Vc(t) when coordinated with the previous gate wire voltage Vs(t) and the current gate wire voltage Vg(t), can yield a flat rectangular voltage V(t)-Vc(t) across the liquid crystal (C_{LC}). This scheme involves a complicated modulation scheme

coordinating modulation voltages at gate wires in relation to the modulation of the voltage at the common electrode in order to achieve their desired flat rectangular modulation of voltage across the liquid crystal.

SUMMARY OF THE INVENTION

The present invention provides various methods and apparatuses for controlling a voltage on an electrode which is used to alter the state of an electro-optic material, such as a liquid crystal layer, such that display data cannot be viewed even if pixel electrodes contain pixel data thereon and for establishing a reference voltage on the pixel electrodes before new pixel data is loaded on the pixel electrode. This control voltage on the electrode is typically provided in a controlled phase relationship relative to the update of pixel data in order to achieve, at least in some embodiments of the present invention, frame-to-frame independence, even at high rates of display. The ability to control the voltage on the electrode in a controlled phase relative to the update of pixel data and the ability to establish a reference voltage on the pixel electrodes before new pixel data is loaded improves, in at least some embodiments, the speed of the display rate and yet retains good frame-to-frame independence.

A display system in one embodiment of the present invention includes a first substrate having a first plurality of pixel electrodes for receiving a first plurality of pixel data values representing a first image to be displayed and also includes an electro-optic layer which is operatively coupled to the pixel electrodes and a control device which is coupled to at least one of the pixel electrodes and an electrode operatively coupled to the electro-optic layer. This display system displays the first image and then applies a first control voltage to the electrode to alter a state of the electro-optic layer such that the first image is substantially not viewable and thus not displayed, and then the display system displays a second image represented by a second plurality of pixel data values after the electrode receives a second control voltage. The control device applies a first reference voltage to the at least one pixel electrode before the display system displays the second image. In many embodiments, the pixel electrodes receive the first reference voltage before the second plurality of pixel data values is loaded onto the pixel electrodes. Typically, the first reference voltage is applied to the pixel

electrodes while the first image is substantially not viewable due to the first control voltage on the electrode.

Typically, at least in some embodiments of the present invention, the electro-optic layer is a liquid crystal layer and the electrode is a common cover glass electrode. This common cover glass electrode and the first substrate forms a structure around the liquid crystal layer such that the first substrate is below the liquid crystal layer and the common cover glass electrode is above the liquid crystal layer. At least in some embodiments, the first control voltage causes the liquid crystal layer to alter its light altering state to turn the display "dark" even if pixel data on the pixel electrodes is still present and would otherwise cause the display to appear white or some other color other than black. After the display is kept at a state such that the first image is not viewable, then the display system displays a second image by causing the electrode to receive a second control voltage which releases the liquid crystal material from its state in which substantially no display data is viewable. Before the display system displays the second image, the pixel electrodes are set to a reference voltage by a control device and then the new pixel data is loaded onto the pixel electrodes so that the second image can be displayed.

There are numerous alternative embodiments of the present invention. For example, the cover glass electrode may exist in separate segments and these segments may be controlled separately such that while one segment is displaying a portion of an image, the other segment is being loaded with pixel data for another portion of the same image and at the same time this other portion is not displaying data because its control electrode in that segment is causing the liquid crystal material in that segment to obscure the data such that it is not viewable.

The present invention may be used in either time sequential color systems or in color systems which employ a triad of subpixels for each pixel. Moreover, the present invention may be employed with or without frame buffering for the next frame while the current frame is being displayed, where this frame buffering may be provided in pixel buffers which are disposed in the same substrate which includes the pixel electrodes. Moreover, the present invention may be used in liquid crystal display devices which are of the reflective type, or alternatively may be used in liquid crystal display devices which are of the transmissive type. Furthermore, the electrode modulation of the present invention may be employed

in a system wherein the electrode which performs the modulation (in order to drive the liquid crystal to a state in which display data is not substantially viewable) is disposed in the same substrate as the pixel electrodes. The present invention in certain embodiments may also include compensating electrodes disposed in the same substrate with the pixel electrodes which compensate for the action of the control electrodes which are causing the display to be not viewable according to certain embodiments of the present invention.

At least some embodiments of the present invention provide various advantages which are described below, although it will be appreciated that certain embodiments of the present invention may only provide some, if any, of these advantages depending on the implementation of the embodiment. For example, the present invention may be used to provide for a display system in which the pixel outputs on the display are simultaneously updated with new data rather than being updated on a row-by-row basis when no frame buffering is used. Moreover, the invention may be used to provide a display system in which there is high frame-to-frame independence, even at high frame rate frequencies. Another advantage of the present invention, at least in some embodiments, is that by simultaneously varying the voltage which drives the control electrode and the voltages which drive the pixel electrodes, a larger average voltage difference can be achieved across the layer of electro-optic material, thereby improving brightness. In another embodiment of the present invention, a voltage greater that the maximum and minimum voltages allowed for driving the pixel electrodes can be used as the control voltage signal applied to the control electrode. This advantage may be useful in a situation where the liquid crystal electro-optic effect has a threshold below which no optical effect occurs. Another advantage of the present invention in certain embodiments is that if the control electrode voltage is modulated with a burst of relatively high frequency oscillation, a dual-frequency liquid crystal display can be driven rapidly.

BRIEF DESCRIPTION OF THE DRAWINGS

The various embodiments of the present invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements.

Figure 1A shows a cross-sectional view and Figure 1B shows a perspective view of an image display system according to one embodiment of the invention.

Figure 2A shows a block diagram representation of a system according to one embodiment of the present invention; this embodiment is a reflective-type liquid crystal display, and it will be appreciated that transmissive-type liquid crystal displays may also be implemented according to the present invention.

Figure 2B shows an electro-optic curve for an example of a normally white liquid crystal.

Figure 2C shows a waveform for a cover glass modulation according to the present invention in conjunction with an intensity versus time graph depicting the behavior of a liquid crystal material under the control of the cover glass waveform also shown in Figure 2C.

Figure 2D shows in further detail a portion of the intensity versus time graph for a liquid crystal under the control of a cover glass electrode or other electrode modulated according to the present invention.

Figures 3A and 3B depict a flowchart illustrating a time sequential liquid crystal display system of the present invention without frame buffering of new pixel data while old pixel data is being displayed.

Figures 4A and 4B depict a flowchart illustrating an embodiment of the present invention which uses time sequential color subframes with frame buffering.

Figure 5 illustrates an embodiment of the present invention which uses a spatial color display wherein each pixel includes three subpixels, each displaying a particular light component.

Figure 6A illustrates an embodiment of a pixel circuit which may be used with the present invention. Figure 6B illustrates an embodiment of a pixel circuit which may also be used with embodiments of the present invention. Figure 6C shows yet another embodiment of a pixel circuit which may be used with embodiments of the present invention. Figure 6D illustrates a pixel circuit having a pixel buffer which is capable of storing the new pixel data value while the old pixel data value is being displayed; the circuit is capable of storing an analog value in the pixel buffer, and it will be appreciated that a plurality of these pixel circuits arranged in an array provides an analog frame buffer.

Figure 7A shows the effects of modulating the electrode voltage modulation with a signal that is not a rectangular waveform, according to an embodiment of the invention in which the upper panel shows the electrode voltage and the pixel electrode voltage with respect to time when an overdrive pulse is applied, and the middle panel shows the voltage across the electro-optic layer (e.g. liquid crystal layer) for such modulation of the electrode and the lower panel shows the intensity output from the pixel A using the overdrive pulse (solid line) and without the overdrive pulse (dashed line).

Figure 7B shows a waveform of the modulation of electrode which may be used to drive the electro-optic layer to a state in which display data is not visible, wherein the waveform uses a reset spike rather than a rectangular pulse. Figure 7C illustrates a waveform for an electrode modulation which may be used to place the electro-optic layer into a state in which the display data is not visible according to one embodiment of the present invention.

Figures 8A and 8B are schematic representations showing waveforms for electrode modulation which include bursts of relatively high frequency oscillation.

Figure 9A is a waveform illustration indicating the electrode modulation voltages and the pixel electrode voltages over time using a frame buffering system; the electrode modulation shown in Figure 9A includes a reset pulse which is designed to place the electro-optic layer into a state in which the display data on the pixel electrodes is not viewable. Figure 9A also shows the intensity of certain pixels over time relative to the waveforms shown in Figure 9A.

Figure 9B illustrates a plurality of intensity versus time waveforms which illustrate the behavior of pixels in a time sequential color display system of the present invention which utilizes electrode modulation such that the electro-optic layer is placed in a state for a certain period of time in which the display data is not viewable.

Figure 10A illustrates an alternative embodiment of a cover glass electrode which has been segmented according to one embodiment of the present invention; other similar embodiments include the use of segmented control electrodes in the same substrate which include the pixel electrodes.

Figure 10B and Figure 10C illustrate a flowchart showing a time sequential color system having segmented control electrodes, such as segmented cover glass electrodes according to one embodiment of the present invention.

Figure 11 illustrates a plurality of waveforms in a time sequential color system having segmented control electrodes.

Figure 12 shows in further detail a time sequential color system having a segmented control electrode for modulating a portion of the electro-optic layer.

Figures 13A, 13B, and 13C illustrate various intensity versus time waveforms for various embodiments employing segmented electrodes for controlling a portion of the electro-optic layer.

Figure 14 shows another embodiment employing segmented electrodes and pulses of illumination rather than continuous illumination.

Figure 15 shows another embodiment employing segmented control electrodes employing pulses of illumination.

Figure 16A shows a pixel circuit according to an embodiment of the present invention which employs compensating electrodes.

Figure 16B shows a top view of a circuit layout of a pixel circuit according to one embodiment of the present invention having a compensating electrode in the pixel circuit in the same substrate as the pixel electrode.

Figure 16C illustrates a voltage versus time graph indicating the waveforms of pixel electrodes and the control electrode voltage which is used to modulate the electro-optic layer to drive it to a state in which display data is not visible.

Figure 16D illustrates the effect of a compensating electrode by showing the various waveforms of the pixel electrodes relative to the compensating electrode voltage and the control electrode voltage which is used to modulate the electro-optic layer.

Figure 16E shows a voltage versus time graph and a time related pixel intensity versus time graph according to one embodiment of the invention.

Figure 17 illustrates control electrode modulation in a display system having frame buffering, such as analog frame buffering using a circuit such as that shown in Figure 6D.

Figure 18 illustrates a voltage versus time waveform of an electrode modulation signal which employs an offset in order to effect the electro-optic layer of the present invention; this embodiment may be used with analog frame buffering or other frame buffering which allows storage of new pixel data in the

same substrate which includes the pixel electrodes which are causing the display of old pixel data.

Figure 19 illustrates a flowchart of one embodiment of the present invention in which pixel electrodes are set to a voltage level before loading pixel data during a reset of the liquid crystal material.

Figure 20 shows a group of waveforms which show the operation of one embodiment of the invention in which pixel electrodes are set to a voltage level before loading pixel data.

Figure 21 shows a schematic of an integrated circuit display device having an array of pixel cells and supporting circuitry, where the display device operates according to one embodiment of the invention in which pixel electrodes are set to a voltage level before loading pixel data.

Figure 22 shows another example of an integrated circuit display device having an array of pixel cells and supporting circuitry, where the display device operates according to one embodiment of the invention in which pixel electrodes are set to a voltage level before loading pixel data.

DETAILED DESCRIPTION

The following description provides examples of the present invention. It will be appreciated, however, that other examples of the present invention will become apparent to those in the art upon examination of this description. Thus, the present description and the accompanying drawings are for purposes of illustration and are not to be used to construe the invention in a restrictive manner.

Figure 1A shows a cross-sectional view of a display system 12 according to one embodiment of the present invention, in which an electro-optic layer 22 is disposed between a first substrate 20 and a second substrate 24. First substrate 20 has a single control electrode known as a common electrode 26 or a cover glass electrode 26. The second substrate has a plurality of pixel electrodes 28 each of which periodically acquires updated image data in an independent manner. Each pixel electrode 28 retains the image data required for a given period of time or duration, after which the acquired image data is replaced with new image data. A voltage applied to each pixel electrode relative to a voltage on the common electrode 26 will cause a voltage to appear across the liquid crystal material (V_{LC}) which will then control the light altering properties of the liquid crystal such that

the liquid crystal may be selectively placed in at least two light altering states. Typically these states include either allowing light to pass through the display system or not allowing the light to pass through the display system. At least one of the first substrate 20 and the second substrate 24 is transparent or translucent to light. According to one embodiment of the invention, the electro-optic layer 22 may comprise liquid crystal material, and the display system 12 may comprise a liquid crystal display. It will be appreciated that other layers may also be present in the structure of the display system 12, such as alignment layers or optical coatings (e.g. anti-reflective coatings)) and that other layers may be used with the display system 12, such as a polarizing layer or layers. Figure 1B shows a prospective view of the same display system shown in Figure 1A. The display system 12 may be a thin film transistor (TFT) system which may be a transmissive type liquid crystal display device or it may be a reflective type liquid crystal display device such as a liquid crystal on silicon substrate device, such as that described in U.S. Patent 5,426,526, which is hereby incorporated herein by reference.

Figure 2A shows a display system 101 according to one embodiment of the present invention. This embodiment employs a reflective type liquid crystal on silicon display system which includes pixel driver logic 102, pixel electrodes 104, a liquid crystal layer 106, and a cover glass electrode 108. The system also includes clock control logic 112, an electrode control driver 110, as well as illuminator 114 and the illuminator control logic 116.

In the system 101, the illuminator 114 may provide white light in the case of a spatial colored display system or it may provide in a controlled time sequence three different color lights (e.g., a red light, and then a green light, and then a blue light each provided separately). The illuminator 114 provides this light 118 through the control of the illuminator control logic 116 which receives clocking signals or control signals 117 from the clock control logic 112. The clock control logic 112 also controls the electrode control driver 110 in order to provide the proper modulated control signal waveforms 111 to the cover glass electrode 108. At the same time, control clock logic 112 also provides clocking signals to the pixel driver logic 102 or it may receive signals from the pixel driver logic 102 in order to coordinate a controlled phase relationship between the control voltage signals applied to the cover glass electrode and the timing of loading and displaying of pixel data onto and through the pixel electrodes 104. The various

modes of operation of this system 101 will be described below according to the various embodiments of the present invention.

Figure 2B shows an intensity versus voltage graph displaying an electro-optic curve for a normally white liquid crystal cell configuration. This curve 125 has the highest intensity at the lowest voltage, which may be zero volts. That is, the light altering state of this liquid crystal is such that the most light is transmitted through the liquid crystal at this lowest voltage state. As the voltage across the liquid crystal increases, the intensity of the light transmitted through the liquid crystal decreases to the point where no light is transmitted at voltage point 127 which has been referred to as the holding to black voltage or V_B 127. According to the present invention, an electrode, such as the cover glass electrode, may be applied a voltage relative to the voltages on the various pixel electrodes such that throughout the liquid crystal layer or at least segments thereof, the voltage across the liquid crystal layer is at or exceeds V_B. According to certain embodiments of the present invention, the voltage applied to this control electrode may be such that the voltage across the liquid crystal is at point 129, which is an overdrive voltage or V_{OD}. This overdrive voltage may be used to rapidly drive the liquid crystal display material to a state in which light does not transmit through it such that the display data is otherwise not viewable even if the display data is stored on the pixel electrodes.

Figure 2C shows two time related graphs which indicate the relationship between the control voltage applied to the control electrode, such as the cover glass electrode, and the intensity of the pixels in a liquid crystal display of the present invention. The voltage waveform 151 of Figure 2C shows the control signal applied to the electrode, and the intensity waveforms 152 of Figure 2C shows the corresponding intensity waveforms at the corresponding times. At time t_0 the voltage applied to the electrode (shown, for example, as V_{CG} in the example where the electrode is the cover glass electrode) is ramped up to a point at which the voltage across the liquid crystal is at least at V_B. This causes the intensity of the pixel to drop rapidly as shown by the pixel intensity curve 153. Then between the times t_0 and t_1 the next pixel display data may be loaded onto the pixel electrode while the display is held in a state in which display data is not visible due to the voltage applied to the control electrode such that the voltage across the liquid crystal (V_{LC}) is at or exceeds V_B. At time t_1 the voltage on the control electrode is

reduced, as shown in the voltage waveform 151, such that the voltage across the liquid crystal is less than V_B. At this point, it is now possible to display and view the pixel data because the pixel electrodes can now control the state of the liquid crystal. At this point beginning at time t_1, the liquid crystal begins to return to a light altering state as shown by the pixel intensity curve 154. Typically, the liquid crystal material will be relaxing to a light altering state which allows more light to pass through. As shown by the pixel intensity curve 154, the liquid crystal may continually relax throughout the entire time period t_1 through t_2 and may not "plateau" or otherwise reach a steady state. This effect will be discussed further below, but it will be noted that with the present invention this is not necessarily a disadvantage because all such pixels may be producing the same effect and yet the viewer can still see the various gradations of color or gray-scale in the image. At time t_2, a first control voltage is again applied to the control electrode such as the cover glass electrode to again drive rapidly the liquid crystal material to a state in which the display data is not visible as shown in the waveform 152 between times t_2 and t_3. At time t_3, the voltage on the control electrode is changed from the first control voltage to a second control voltage such that display data may be visible as shown by the pixel intensity curve 155 between times t_3 and t_4. It will be appreciated that the control voltage waveform 151 which is applied to the control electrode is a DC balanced signal (around some level) and that over time it averages to that DC level. It will be appreciated that the present invention may be used with DC balanced control signals or without DC balanced control signals, but that there are advantages of using DC balanced control signals.

Figure 2D shows in further detail one frame or subframe of a method of the present invention. In particular, a pixel intensity waveform 160 is shown in Figure 2D as having three portions or curves 161, 162, and 163. Curve 161 illustrates the rapid drive to black of the liquid crystal material upon the application of a control voltage to the control electrode which causes the voltage across the liquid crystal to be approximately equal to V_B. During the time in which this control voltage is applied to the control electrode, the pixel intensity is at its lowest as shown by curve 162. It will be appreciated that rather than driving the liquid crystal material entirely to black, the liquid crystal may be driven substantially to a dark state such that the image may be barely discernible. In this alternative embodiment, there still may be substantial benefits derived from driving a liquid

crystal state such that the display data is substantially not viewable in order to achieve frame-to-frame independence. During the time between t_0 and t_1, the next pixel data may be loaded into the pixel electrode as indicated by the time T_L. This is also the time during which the display is kept in its dark state by keeping the voltage across the liquid crystal preferably at or above V_B. At time t_1, the control voltage on the control electrode is released to a second control voltage such that the voltage across the liquid crystal changes, thereby allowing the liquid crystal to relax to various light altering states and allowing display data to be viewable. This is shown by the pixel intensity curve 163 which indicates the intensity of the pixel rising as the liquid crystal continues to relax during the relaxation time designated as TLC which occurs between times t_1 and t_3. According to various embodiments of the present invention, it may be desirable to provide illumination during the entire time from t_1 to t_3 or only a portion of the time such as that shown in Figure 2D. In particular, Figure 2D shows illumination of the pixel only during the times t_2 through t_3. In another embodiment, pulses of light during portions of time within the period t_2 through t_3 may be provided rather than continuously illuminating the display from time t_2 through t_3. The frame or subframe cycle ends at t_3 when the first control voltage is again applied to the control electrode such that the voltage across the liquid crystal is substantially at V_B (or preferably at or above V_B).

Figures 3A and 3B show a particular method of the present invention which is used in a time sequential color display system without any frame buffering in pixel buffers associated with pixel electrodes on the same substrate. Figures 4A and 4B show a similar system but with such frame buffering. The method shown in Figures 3A and 3B will be described first.

The method 200 may be considered to begin in step 202 in which "old" pixel data may be displayed from the last subframe of the prior frame of display data. Following the end of that display time, in step 204, the cover glass voltage is set by applying a first control voltage to alter the state of the liquid crystal so that the old pixel data is substantially not viewable, even if some of the pixel data is still stored on the pixel electrodes. Typically, the first control voltage applied to the control electrode such as a cover glass electrode is such that relative to the pixel electrode voltages, there will be at least V_B volts across the liquid crystal. In step 206, the next pixel data is loaded onto the pixel electrodes for the first color

subframe for the current frame while continuing to hold the voltage of the control electrode substantially at a voltage so that the voltage across the liquid crystal is at least at V_B. In this manner, the pixel electrodes are loaded with new data while the display is kept substantially dark. It will be appreciated that typically the data is loaded row by row of the pixel electrodes which correspond to rows on the display, one row at a time. Next, in step 208, the voltage on the control electrode is changed in order to release the state of the liquid crystal so that the loaded next data for the first color subframe (which was loaded in step 206) is now viewable on the display. If all the rows of the display have been loaded before releasing the voltage on the control electrode, then the display appears to update simultaneously for the whole frame. Then in step 210 the first color subframe is displayed for some time. One advantage of the prior sequence of steps is that there is a period of darkness between the old frame and the new frame such that now the frames have more frame-to-frame independence and hence the image appears better to a user. Moreover, even though the pixel data was loaded row by row onto the electrodes rather than simultaneously onto the electrodes for one frame, the display will still appear to update simultaneously for the whole frame because the releasing of the voltage on the control electrode at one time causes the liquid crystal to suddenly be able to change its "pixel" states for the whole liquid crystal layer simultaneously for the whole frame. The simultaneous nature of the liquid crystal's response provides a major advantage because it means that the liquid crystal does not have to complete switching (from a prior light altering state to a new light altering state) before it can be illuminated. Thus, the display system can be illuminated before the liquid crystal finishes switching (or completing its trajectories) and yet the display will still appear uniform across the display. Another advantage of this invention is that, because the liquid crystal is not, at least in some embodiments, required to complete its switching to a saturated state, the appearance of the display becomes less sensitive to variations in the thickness of the liquid crystal. This improves the apparent uniformity of the display. The fact that the liquid crystal is switched from an unsaturated state of the liquid crystal at the end of a display cycle (shown for example by pixel intensity curve 154 in Figure 2C) means that display frame rates may be increased (e.g. increasing the frame rate from 30 Hz to 60 Hz) which improves the appearance of the display.

Next in step 212 the voltage on the control electrode is again set (e.g. by applying the first control voltage) to alter the state of the liquid crystal so the data for the first color subframe is substantially not viewable (even if pixel data for the first color subframe is stored on some pixel electrodes). Next in step 214, the next pixel data is loaded onto the pixel electrodes for the second color subframe for the current frame while maintaining the voltage on the control electrode so that the voltage across the liquid crystal is substantially or approximately at V_B. In step 216, the second control voltage is applied to the control electrode to allow the liquid crystal to relax so that the loaded data for the second color subframe is viewable on the display. Then in step 218 the second color subframe is displayed for some time. Typically this will include illuminating the display either with continuous illumination or with pulses of illumination as described herein. In step 220 the liquid crystal is again driven to a state in which the pixel data is not viewable. In this case, the data for the second color subframe is made to be substantially not viewable, even if the pixel data for the second color subframe remains stored on some of the pixel electrodes. Then in step 222, the next data is loaded onto the pixel electrodes for the third color subframe for the current frame while holding the voltage on the control electrode so that the voltage across the liquid crystal is substantially at V_B. Then at step 224, the voltage on the control electrode is released (e.g. applying a second control voltage) to alter the state of the liquid crystal so that the loaded data for the third color subframe for the current frame is now viewable on the display. Then in step 226, the third color subframe is displayed while illuminating the display system. It will also be appreciated that a similar illumination step may occur in step 210. In step 228, the method repeats steps 204-226 (inclusive) again for the next display frame. This continues for each frame as data is supplied to the system.

The method 425 shown in Figures 4A and 4B is similar to the method 200 except that the system of this embodiment uses a pixel frame buffer to store the next frame of pixel data while displaying the current pixel data. That is, while the display step occurs, the pixel buffers which will store the next pixel data are being loaded during the displaying of the current frame. Typically, this may be implemented in a system where the pixel buffer for a particular pixel electrode is located substantially under the pixel mirror electrode. This is described in further detail in U.S. Patent 5,426,526. A particular pixel circuit for performing the

pixel-by-pixel frame buffering in a pixel buffer associated with its respective pixel electrode is shown in Figure 6D herein.

The method 425 begins at step 427 in which old pixel data from the last subframe of the prior frame of display data is displayed; while displaying this old pixel data, data for the first color subframe of the next frame is loaded into a pixel buffer for each pixel. According to one embodiment of the present invention, the pixel buffer stores analog pixel information, and the circuit of Figure 6D may be employed for this purpose. In step 429, the control electrode, such as the cover glass electrode, is set at a voltage (e.g. by applying a first control voltage) to alter the state of the liquid crystal so that the old pixel data (for the last subframe of the prior frame) is substantially not viewable. Also during this step 429, for each pixel, buffered data stored in each pixel buffer for the first color subframe is loaded from the pixel buffer onto the pixel electrode. In step 431, the voltage on the control electrode is altered so that the state of the liquid crystal may relax thereby allowing the loaded pixel data for the first color subframe to be viewable on the display. If all the rows of the display have been loaded before releasing the control electrode by applying the second control voltage, then the display appears to update substantially simultaneously for the whole frame. Typically, with a frame buffer capability of the system described herein one would normally load all rows of the display although this is not necessarily required for certain embodiments of the invention. In step 433, the first color subframe is displayed and while displaying the first color subframe, data for the second color subframe is loaded into a pixel buffer for each pixel. In step 435, the control electrode, such as the cover glass electrode, receives the first control voltage which alters the state of the liquid crystal so that data for the first color subframe is substantially not viewable; also during this step 435, buffered data for the second color subframe which has been loaded into the pixel buffers is now loaded from the pixel buffer onto the pixel electrode. In step 437, the voltage on the control electrode is changed to "release" the liquid crystal from the state in which it was held in step 435 so that the loaded data for the second color subframe is viewable on the display. In step 439, the second color subframe is displayed and while displaying the second color subframe, data for the third color subframe is loaded into a pixel buffer for each pixel. In step 441, a first control voltage is applied to the control electrode, such as the cover glass electrode, in order to alter the state of the liquid

crystal so that data for the second color subframe is substantially not viewable; also during this step 441, pixel data for the third color subframe is loaded from the pixel buffer of each pixel onto the corresponding pixel electrode of each pixel. In step 443, the voltage on the control electrode is changed (e.g. by applying the second control voltage) to alter the state of the liquid crystal so that the loaded data for the third color subframe for the current frame is viewable on the display. Then in step 445, the third color subframe is displayed, and while displaying the third color subframe of the current frame, data for the first color subframe for the next frame is loaded into a pixel buffer of each pixel. In step 447, the method repeats steps 429-445 (inclusive) for the next display frame and this continues for each display frame which is received by the display system of the present invention.

Figure 5 shows a method 500 according to another embodiment of the present invention. This embodiment utilizes a system having a spatial color first substrate, wherein for each pixel there are three subpixels which provide the three signals for three primary colors, such as red, green and blue. These spatial color systems are well known in the prior art. The present invention provides an advantage in these systems in that simultaneous update may be achieved while also providing frame-to-frame independence without having to incorporate a pixel buffer for each pixel to thereby provide a frame buffer on the same substrate with the pixel electrodes. Method 500 begins in step 502 in which "old" pixel data from the prior frame of display data is displayed in the display system. Then in step 504, the control electrode receives a control voltage which alters the state of the liquid crystals such that the old pixel data is substantially not viewable even if the pixel data is stored on at least some of the pixel electrodes. As a result, typically in most embodiments of the present innovation the display frame is momentarily driven dark. In step 506, the next data for each pixel is now loaded onto the pixel electrodes in a row-by-row manner as in the prior art for the current frame while continuing to keep the voltage on the control electrode substantially at a voltage so that the voltage across the liquid crystal is preferably at or above V_B. Then in step 508 the voltage on the control electrode is changed to the second control voltage to thereby allow the liquid crystal to change its state so that the loaded next data (loaded in step 506) for the current frame is now viewable on the display. If all of the rows of the display have been loaded before releasing the voltage on the control electrode, then the display appears to update simultaneously

for the whole frame even though the pixel electrodes were updated simultaneously only on each row at a time. Then in step 510, the current frame is displayed for some duration. Step 512 involves the repeating of steps 504-510 (inclusive) for the next display frame. In this manner, a spatial color display system may achieve improved frame-to-frame independence while at the same time achieving simultaneous update for the whole frame without having frame buffering on the same substrate as the pixel electrodes.

Figures 6A, 6B, 6C and 6D show various pixel circuits which may be employed with the present invention. For example, the circuits of Figure 6A, 6B, and 6C may be employed where no frame buffering on the pixel electrode substrate is required. Each of these circuits include at least one pixel electrode, such as pixel electrodes 651, 661, or 671, and further include control transistors which are used to selectively load the pixel electrode. These control transistors are shown as FET's 652 of Figure 6A, 662 and 663 of Figure 6B, and 674 of Figure 6C. The operation of these pixel circuits is well known in the art, and it will be appreciated that there is an array of such circuits wherein the array includes a plurality of rows of the pixel circuits where each row includes a plurality of columns of the pixel circuits.

Figure 6D shows a pixel circuit which may be used with certain embodiments of the present invention which require pixel buffering in pixel buffers located on the same substrate with the pixel electrodes. The pixel circuit of Figure 6D includes a conventional row select wire 687 and a data or column wire 686 and also includes a control or pass transistor 685. This pixel circuit further includes a pullup FET 682 and a pulldown FET 683 as well as a voltage follower FET 684. This pixel circuit of Figure 6D operates in the following manner: while old pixel data values are being held or stored on the pixel electrode 681 (with the pulldown signal 688 being kept low such that the FET 683 is off) a new pixel data value is loaded into the pixel circuit or cell by applying a high row select signal on row select wire 687 and concurrently applying the pixel data value on data wire 686. In this condition, the FET 685 passes the pixel data value, which is preferably an analog pixel data value, through to the gate of the FET 684 which should not be in a conducting state at this point since the pullup signal is kept low so that substantially no current is flowing through the source/drain electrodes of either FET 682 or FET 684. After loading the next pixel data value onto the gate

of FET 684, the FET 685 is turned off by driving the row select wire 687 low. This will keep the new pixel data value stored on the gate of FET 684 while data wire 686 applies another new pixel data value to a pixel cell in the same column but a different row. Then, near the end of the display of the old pixel value on pixel electrode 681, the pulldown signal 688 is asserted high, thereby turning on FET 683 which then discharges any charge on the pixel electrode 681. Then the pulldown signal 688 is turned low again to turn off the FET 683 and then the pullup signal is asserted high to turn on the FET 682. This causes the FET 684 to pull up its source node which is coupled to the pixel electrode 681 to within one threshold value of the pixel data value (preferably an analog pixel data value) stored on the gate of the FET 684. After this pullup occurs, the pullup signal is deasserted to a low value to cause no current flow through the FETs 682 and 684 thereby allowing the value stored on the pixel electrode 681 to control the display state of the liquid crystal in the proximity of the pixel electrode 681. It will be appreciated that an array (in rows and columns) of pixel circuits of the type shown in Figure 6D will provide, in one embodiment, an analog frame buffer in the same integrated circuit (monocrystalline silicon) substrate as the pixel electrodes. Moreover, each such pixel circuit may be fabricated such that it is disposed under each pixel electrode, which in one embodiment may be a reflective mirror for a reflective type liquid crystal display.

Figure 7A shows an example of a liquid crystal pixel switching between gray levels or color levels. This figure depicts the optical response from a single pixel (pixel A) switching between levels over three frame periods. In this example, the liquid crystal is driven toward a bright state by increasing voltage, and the DC balance is affected on a frame-by-frame basis. The figure shows the effects of modulating the common electrode voltage modulation with a pulse which is designed to alter the light altering state of the liquid crystal such that display data is not usefully viewable. In this instance, rather than being driven dark, the display is driven whiter and yet the display data is not usefully viewable as the whole display will be driven brighter. It will be appreciated that it will generally be preferable to not illuminate or view the display during the state in which the display is driven whiter by the pulses 401.

Referring to Figure 7A, the upper section of this figure shows the voltages at the control electrode or common electrode and the pixel electrode voltage with

respect to time when the pulse 401 is applied. The middle section of Figure 7A shows voltage across the liquid crystal for such modulation of the common electrode voltage, and the lower section of Figure 7A shows the intensity output from pixel A with the pulse 401 and without the pulse 401 (where the response without the pulse 401 is shown by the dashed line). The pulse 401 need not be limited to a flat pulse, and it can be positive or negative with respect to ground and can even alternate between positive and negative as shown in Figure 7A. It will be appreciated that this pulse is similar to the pulse on the voltage waveform 151 which occurs between times t_0 and t_1 of Figure 2C.

The amplitude and duration of the pulse 401 of Figure 7A at the beginning of a frame period are chosen such that the pulse momentarily drives the liquid crystal beyond the target gray value. For sequential display as described above, the duration of the pulse can be from a fraction of a millisecond to over one millisecond and the amplitude can be any value that yields a pulse 405 with a voltage level V_{LC} across the liquid crystal layer which is sufficiently large to produce an intensity surge 409 at pixel A. In an alternative embodiment, of course, the liquid crystal may be driven dark rather than driven bright. Since the pulse 401 is applied to all pixels which share the electrode, it results in an increased switching time between one gray level and a lower gray level. It has the advantage that the time switching between one gray level and a slightly increased gray level is not limited by the observed delay, and slow response in such situations (this is indicated by the dashed line in Figure 7A). Indeed, the upper limit for the time taken for any transition is now bounded by the relaxation time after the pulse. One consequence of this pulse is that, depending on its polarity, the voltage across the electro-optic layer may be momentarily (transiently) increased or decreased immediately following that pulse. In one embodiment, the additional or superimposed pulse may be temporarily close to the update or acquisition of image data on the pixel electrodes.

Figure 7B shows another approach to modulating the control electrode, such as a common cover glass electrode for a sequential display device using a pulse with a voltage that peaks with an exponential type decay. The pulse may, for example, be added near the time at which all the pixels are updated.

Figure 7C shows another alternative embodiment for modulating the voltage on the control electrode. The modulation pattern 461 has a voltage

waveform 462 that includes several components as shown in this voltage versus time diagram. A frame cycle begins at time t_0 in which the voltage on the control electrode is ramped to a high enough voltage such that V_{LC} is driven close to V_{OD} (see Figure 2B). This voltage state continues during the duration between time t_0 and time t_1. This causes the liquid crystal to be rapidly driven to a state in which the display data is not viewable. Then from time t_1 to t_2, the voltage on the control electrode is changed so that instead of overdriving the liquid crystal layer, it is held at a voltage such as V_B (see Figure 2B). The time from time t_0 to t_2 may be utilized by the display system to load all the pixel electrodes with new display data for the current frame (and effectively erasing the old display data) then at time t_2 the pixel data may begin to be displayed. Typically, all pixel electrodes would have been loaded by the beginning of time t_2 and thus all liquid crystal can begin the transition from the altered state which existed during the time between t_0 and t_2 to a relaxed state. The relaxation of the liquid crystal is allowed to occur between times t_2 and t_3 which is also the time in which the image data is being displayed at least part of this time period. Typically, the time between t_2 and t_3 includes illumination of the display for at least a portion of the time if not all the time. Moreover, rather than illuminating continuously through a portion of the time between t_2 and t_3, pulses of illumination may be applied. The modulation scheme of Figure 7C thus achieves an advantage of rapidly driving the crystal to an altered state in which the display data is not viewable while then relaxing it but still keeping it not viewable. This increases the response time of the device thereby allowing the frame rate of the display device to be driven at higher frequencies, subject to the amount of time it takes to load the pixel electrodes in the frame. The cycle beginning at time t_3 continues except the polarity of the signals has changed due to the fact that the control voltage signal applied to the control electrode is DC balanced around some DC level (shown here as some level other than zero volts). It will be appreciated that DC balancing is performed in order to attempt to provide a DC balanced signal to the liquid crystal such that the DC balance level of the liquid crystal is approximately zero volts.

Figures 8A and 8B illustrate another embodiment of the present invention in which the control voltage which is applied to the control electrode is modulated with a burst of a relatively high frequency oscillation (e.g. 5kHz to 100kHz). Such a scheme would be useful for driving dual-frequency liquid crystal materials

in those types of displays where below the crossover frequency the liquid crystal material has a positive dielectric anisotropy, and above the crossover frequency it has a negative dielectric anisotropy.

As an example of the usefulness of a display system featuring such a scheme, consider the following scenario. An image is written to display system 12 by applying a pattern of voltages to the array of pixel electrodes 28. Common electrode 26 is modulated according to an embodiment of the invention as described above, or alternatively, may be clamped at a given voltage while each pixel of electro-optic layer 22 switches to the desired state. Then after the image has been viewed, it is desired to rapidly reset each pixel of the electro-optic layer 22 to an off state in preparation for the acquisition of the next set of image data such that the old image data is not viewable while acquiring the new set of image data or if acquired already, may be separated from the prior frame by momentarily blanking the display. This can be achieved by using a dual-frequency electro-optic liquid crystal material and performing this reset, or drive to off function, by applying a short period of high frequency voltage signal to the common electrode 26. It will be appreciated that if an AC signal is used to hold the liquid crystal to a state in which the display (pixel) data is substantially not viewable (e.g. a "dark" state), then it is preferred to synchronize the phase of the AC signal with the phase of writing pixel data to each row of pixel electrodes so as to equalize between rows the effect of capacitive coupling between the control electrode (e.g. the common electrode) and the pixel electrodes.

Within the basic scheme for electrode modulation of the present invention, in which the electrode voltage has a close temporal relationship with the update of image data to the pixel electrodes, there exists a number of variations concerning the nature of the modulation. For example, in one embodiment of the invention, relatively short pulses may be applied to an otherwise DC control electrode voltage. Here the modulation may consist of pulses of shorter duration than that of the image data on the pixels. In another embodiment of the control electrode voltage modulation scheme according to the present invention, the pulse duration applied to the control electrode may be of longer duration than that of image data on the pixels. In this latter case, the time period with which the image data remains on the pixels is shorter that the refresh period.

According to another embodiment of the invention, the control electrode voltage modulation may comprise bursts of relatively high frequency alternating current (AC) modulation. In another embodiment, the control electrode voltage modulation may comprise one burst of relatively high frequency modulation for each update of image data to the pixel electrodes.

As shown in Figure 9A, according to a further embodiment of the present invention, the common electrode voltage can be modulated with a pulse to achieve a rapid "drive to dark" of the electro-optic material or liquid crystal despite any pixel data stored on the pixel electrodes during the drive to dark state. Certain liquid crystal cell configurations can be constructed which are normally white, and require addressing by a voltage to drive the cell to a dark state. According to this embodiment, this voltage addressing can be done by driving the common electrode to a voltage sufficiently different from the pixel voltage to achieve a rapid drive to dark. Gray or color levels are subsequently established by allowing the liquid crystal to relax back and generate different gray or color levels depending on the voltage on the pixel electrode. It will be appreciated that gray may be considered a color for the purposes of the present invention. The embodiment shown in Figure 9A also utilizes a pixel frame buffer which stores the next pixel data in a pixel buffer while the current pixel data is being displayed.

The common electrode voltage can be over driven to get the electro-optic material very quickly to a dark state by using a voltage greater than the voltage required to hold a dark state.

An example of an electro-optic response which would be suitable for this embodiment is shown in Figure 2B. The intensity output from a pixel decreases with the voltage applied across the electro-optic layer. The electro-optic curve shown here has a saturation response as the voltage is increased above the "black holding voltage", that is, the output remains dark for higher voltages. The present invention may also be used with liquid crystals having different electro-optic curves, such as one which is similar to that shown in Figure 2B except that the curve 125 begins to rise again at some point after point 127 (e.g. perhaps before V_{OD}) rather than remaining flat, in which case V_{OD} would not normally be applied to such a liquid crystal. Alternatively, a thick liquid crystal layer may be used which has a more complex curve, which curve 125 may be considered to be a portion of; in this case of a thick liquid crystal, the useful portion of the curve 125

may be used without allowing the crystal to relax completely to other portions of the complete, complex curve. It will also be appreciated that, for certain liquid crystals, different electro-optic (EO) curves may exist for different colors (e.g. a liquid crystal may have a first EO curve for one color (with a V_B of V_B EO1) and a second EO curve for another color (with a V_B of V_B EO2)). In this case, it is desirable to coordinate the control voltage applied to the control electrode relative to the color such that the control voltage matches the color and EO curves. In this case, care should be taken to make sure that the V_B across the liquid crystal created by the electrode is sufficient to render the prior pixel data unviewable before the next pixel data is to be displayed.

The relaxation to the gray scales happens through a related family of curves which, even if the material slows down through temperature decrease, will still allow the viewing of gray or color levels. Subsequent images are independent of each other since there is a complete reset of the electro-optic material between each image.

A longer viewing time can be achieved in systems which employ time sequential color illumination or time sequential color filtration because, as the reset cycle makes color subframes independent of each other, the device can be viewed even as the material approaches the final gray or color level for a frame from the dark state. It may also be useful to view the pixels even during the rapid reset phase to gain more light throughput. A color sequential scheme is shown in Figure 9B.

In particular, Figure 9B shows the rapid drive to dark after each color subframe. Each color subframe can have approximately a 5 ms duration in which it is illuminated continuously during the whole duration or continuously only a portion of the duration or illuminated with only non-contiguous pulses of illumination during the duration. A red subframe, green subframe, and blue subframe can be sequentially displayed within approximately 15 ms. These time periods are merely examples of durations that can achieve visual integration according to U.S. Patent applications 08/505,654 and 08/605,999, the contents of which are incorporated herein by reference. It should be understood, however, that other durations could achieve this including subframe display durations less than 5 ms and even durations of 10 ms or more.

Referring to Figures 9A and 9B, a reset pulse 600 is applied to the pixel electrode for a small portion (here 1ms) of the subframe duration (here 5ms). Assume there are four pixels 601, 602, 603, and 604 with respective initial intensities of I1, I2, I3, I4 and with respective intensities of 1-4. Once reset pulse 600 is presented to pixels 601-604, their intensities 1-4 drop from I1-I4 to zero, respectively, i.e., they undergo a rapid drive to dark at time t_1. Note that the display does not show viewable data even though the pixel electrodes have pixel data values thereon. Also note that all pixel electrodes simultaneously receive updated pixel data values (As shown by the immediate and universal change at the very beginning of the pulse 600 and the pulse 609). This is because the display system of Figure 9A uses pixel frame buffering, which is typically implemented by including a pixel buffer (e.g. analog pixel buffer) with each pixel electrode (e.g. as in Figure 6D). The intensities 1-4 then increase to their respective gray color levels after the reset pulse stops. As depicted, pixel 604 is driven to the brightest gray or color level. The brightness of each pixel as it appears to an observer should be proportional to the area under each curve 1-4. A following reset pulse 609 then drives pixels 601-604 to dark at t_2. The following relaxation to gray or color levels is shown with slower intensity versus time transitions as might occur when pixels 601-604 are cold. As can be seen, frame (or subframe) independence is achieved for pixels 601-604 even if the pixels are cool. It will be appreciated that the use of a frame buffer (as in Figure 9A) with the present invention potentially allows a short reset pulse to be applied (to make the prior frame substantially unviewable) without having to hold the reset pulse while the pixel electrodes are loaded. Since an entire frame of pixel data may be loaded from the frame buffer (of pixel buffers) onto the pixel electrodes by applying a load signal (e.g. appropriately applied pullup and pulldown signals as described for the pixel circuit of Figure 6D) to all pixels, the time required for loading of pixel electrodes is much shorter than a non-frame buffer system which is loaded one (or two) rows at a time. Thus, the frame-to-frame independence may be achieved with a shorter reset pulse (and without the need for a longer hold pulse which is required to load the pixel electrodes).

Liquid crystal configurations can be considered which would not normally be suitable for some applications. For example, a thick cell may be easier to manufacture but will likely to have a response which is too slow. By overdriving

to get a fast reset to dark, and then viewing gray scales or color levels as the cell relaxes, good performance can be achieved even if the cell never reaches its final state for that addressing voltage. The reset makes this viable because of frame independence.

This embodiment can be made to work with different types of DC balancing. Frame based, column based, row based or even pixel-by-pixel DC balancing can be implemented simply by clamping the common electrode at $(V_{max}-V_{min})/2$ and ensuring that subsequent drive to dark pulses are of alternate polarity. In that case, the liquid crystal is DC balanced by controlling only the data driven to the pixel electrodes.

Frame inversion DC balancing can also be implemented in a scheme which modulates the common electrode voltage. An example of this is shown in Figure 9A. In general, DC balance can be maintained with this drive to dark scheme by ensuring that the pixel electrode data updates and the drive to dark pulse sequence are arranged so that over a number of update cycles, the voltage across the electro-optic later averages to a value close to zero.

The pixel electrodes can either be clamped at some known voltage during the reset period or they can be left in some arbitrary state if the common electrode drive is sufficiently high voltage.

As shown in Figure 9A and 9B, an initial reset can be applied with all pixels set to zero volts. The electro-optic device, e.g., a liquid crystal device, has all pixels go rapidly to dark. The pixels are then all set to their gray or color level voltages and the liquid crystal display begins to relax to the gray or color level corresponding to those voltages. The device can be viewed through this entire relaxation (and also though the next reset) because this image is not contaminated with the previous one. The next reset is shown with the pixels set to their highest voltage and the common electrode driven negative. The next image is shown with the common electrode set at the maximum pixel voltage and pixel electrodes below that. Hence, in this particular example DC balance is achieved on a frame-by-frame basis.

It is important to note in this embodiment of the present invention that it is possible to achieve essentially simultaneous drive to dark in the optical output of a large group of pixels, such as an image even if the pixels do not have the facility to perform a simultaneous update of their electrodes with new data . Furthermore, it

is possible to make pixels appear to have the facility for simultaneous electrode voltage update by using the present invention.

Figure 10A shows a segmented display 800 made of an array of pixels which in this case have their electrode voltages updated one row at a time (or with a proper array layout, two rows at a time). Pixels 802 and 803 marked "A" and "B" are on a first row 804 of a segment 809 of array 812 and the pixels 814 and 815 marked "C" and "D" are on the last row 806 of segment 809. Second and third segments 810 and 811 of array 812 are also shown. It should be understood that any segmentation of array 812, which includes the pixel electrodes and other pixel cell circuitry, can be made and that resulting segments can have only a few pixels or a larger number of pixels and that these pixels can be in one or more rows. Whatever the segmentation of array 812, electrode 820 is segmented accordingly. Here, for example, electrode segments 831, 832, and 833 are arranged to correspond to first, second, and third segments 809, 810, and 811 (having three groups of pixel electrodes) of display array 812.

Figures 10B and 10C show one embodiment of a method of the present invention using segmented control electrodes in a time sequential color display system of the present invention. The method begins in step 1001 in which normally three steps occur substantially contemporaneously in a preferred embodiment. It will be appreciated that these three steps need not occur substantially contemporaneously and may only partially overlap in time. However, to achieve numerous benefits from this method, it is preferred that these three steps occur substantially contemporaneously in time. These three steps include loading the next pixel data in the second color component (e.g. a red color component) for the first segment of the control electrode onto the pixel electrodes in the first segment. Also included is resetting the first segment to dark by setting the first segment control electrode to a voltage such that the associated liquid crystal material does not allow pixel data to be viewable. At the same time, pixel data in the second segment is displayed with a first light component, such as a blue light component. In step 1003, three processes are typically performed substantially contemporaneously according to the preferred implementation of the present invention. Step 1003 includes loading the next pixel data in the second color component (e.g. red pixel data) for the second segment onto the pixel electrodes in the second segment. Step 1003 also includes resetting the second

segment to dark by applying the proper voltage to the control electrode of the second segment. Also at the same time, pixel data in the first segment is displayed with a second light component, such as red light. Then in step 1005, the system continues to display the first segment of the image with the second light component and begins to display in the second segment the data of the second segment with the second light component which is red as shown in Figure 11. The processes performed in step 1001 occur between times t_0 and t_1 as shown in Figure 11. The processes performed within step 1003 are performed within the times t_1 through t_2 in the waveforms shown in Figure 11. The two display processes of step 1005 are performed during times t_2 through t_3 of Figure 11.

Figure 11 illustrates the action over time according to this method shown in Figures 10B and 10C for five different components of the system of the present invention. In particular, graph 1101 shows the actions taken relative to the pixel electrodes over time by showing the voltage versus time diagram of the pixel electrode and the loading of data onto the pixel electrode over time. Graph 1103 shows the voltage versus time control of the control electrodes having two separate segments in order to reset to dark the different portions of the liquid crystal layer. Graph 1104 shows an intensity versus time graph of a pixel in the first segment of the liquid crystal. Graph 1105 shows the operation of the three different light illuminators over time relative to the operation of the other components of the system as shown in Figure 11. Graph 1106 shows the intensity over time of the liquid crystal in segment 2 of the liquid crystal layer.

Continuing with a description of Figures 10B and 10C, step 1007 comprises three operations which are typically performed substantially contemporaneously. These operations occur during the time period between times t_3 and t_4 as shown in Figure 11. Next, step 1009 is performed in which three operations are performed substantially contemporaneously between times t_4 and t_5 of Figure 11. Then in step 1011, the system continues to display the first segment with the third light component (e.g. green light) and begins to display the second segment with the third light component, such as green light. This is shown as occurring between times t_5 and t_6 in Figure 11. It should be noted that the staggering of the different segments relative to a particular light component, such as a red light component, does not affect the overall appearance of the display as each segment receives an equal amount of display time and an equal amount of

illumination. An advantage of this approach is that while maintaining the same amount of time for the liquid crystal to switch from one light altering state to another light altering state, the time required for loading the pixel data can be approximately doubled, thereby allowing freedom of design with respect to the driver electronics which is loading the pixel electrodes. For example, cheaper, slower electronics could be used rather than faster, more expensive driver electronics.

The method shown in Figures 10B and 10C continues in steps 1013, 1015, 1017, and finally 1019 as shown in these figures. Step 1013 occurs between time frames t_6 and t_7 of Figure 11, and step 1015 occurs during time frames t_7 through t_8 of Figure 11. Step 1017 occurs beyond time t_8 and before the next frame begins which may be considered time t_0.

The method shown in Figures 10B, 10C and 11 assumes the use of two equally sized segments where one segment displays one half of an image and the other segment displays the other half of the image. It can be shown that a two segment display has certain advantages and is therefore preferred for flood illumination. For example, such a display appears to maximize the time allowed for loading of pixel data while at the same time maintaining approximately the same amount of time for the liquid crystal to switch as with a single common control electrode, such as a cover glass common electrode. Flood illumination typically uses a source of light (e.g. one primary color in a time sequential system or "white" light in a spatial color system) which illuminates the entire display device (all segments) rather than some form of structured illumination, such as a scanned light source which illuminates only a portion at a time while the source is scanned across the display. A display system using a segmented filter or structured illumination may require more than two segments.

Figure 12 shows the action of four different pixels, A, B, C, and D relative to the control voltage applied to the control electrode which in the case of the embodiment of Figure 11 is a segmented or partitioned electrode. These pixels A, B, C, and D of Figure 12 are the same as pixels A, B, C, and D shown in Figure 10A. Note in Figure 12 how, during the reset period in which the pixel data is not viewable, the pixel electrodes for pixels A and B are updated substantially simultaneously at the beginning of the reset to dark period because these pixels are on the first row in the segment 804 and yet do not affect the display as shown in

the bottom portion of Figure 12 because of the control voltage applied to the control electrode as described above. Also note how the pixel electrodes for pixels C and D are updated near the end of the reset to dark phase.

The sequence shown in Figure 12 begins with pixels "A", "B", "C", and "D" all having electrode voltages corresponding to an image which has been viewed and is about to be updated. A first segment common electrode voltage at first segment 831 of common electrode 820 is modulated to a high voltage to drive rapidly all the pixels to the dark state, independent of the voltage on the pixel electrodes. The pixel electrodes for pixels 802, 803, and 815 are then updated to their new voltage levels in the conventional one row at a time addressing scheme 831. When all the rows in this segment have been updated the common electrode is set to its next value for image display. In Figure 12 this is shown as zero volts, but the value depends on the choice of DC balancing scheme used. Also, for liquid crystal driving, the drive to dark pulse is likely to alternate between positive and negative pulses to preserve DC balance. Note that all the pixels are driven to a dark state rapidly and simultaneously, and all the pixels begin their trajectory towards a gray level simultaneously, even though the pixel electrode voltages are updated one row at a time. Also note that the system of Figure 12 does not employ pixel frame buffering (e.g. an array of pixel circuits with pixel buffers) as the pixel electrodes are not updated substantially simultaneously, Also, it will be appreciated that Figure 12 also depicts the actions of a display system in which the control electrode is not segmented.

This display system with a segmented control electrode may be used to make all pixels under the segment appear to update simultaneously. This scheme could be used, for example, to generate time sequential color in a system which has a segmented color filter placed over the display, or which uses some form of structured illumination (e.g. scanning illumination rather than flood illumination). Also, the scheme may be used with some form of flood illumination, and this flood illumination may be continuous during a frame or subframe or non-contiguous pulses of illumination may be applied during a frame or subframes. This will be further illustrated with reference to Figures 13A, 13B, 13C, 14 and 15.

It should be noted before discussing the illumination aspects that the present invention provides for a multiple segmented control electrode where there

may be more than two segments. This is shown, for example, in Figure 13A in which there are three segments which are separately loaded onto pixel electrodes and then displayed after releasing the appropriate control electrode for that segment. The embodiment shown in Figure 13A shows an intensity versus time graph of three different pixels in three different segments of the display system . In particular, the graph 1301 shows a liquid crystal switching time t_{LC1} which is under an intensity curve 1304 for a pixel in the first segment. This pixel was loaded during time t_1 shown as time 1303. Pixel intensity curve 1305 represents a pixel in a second segment which would be loaded after time t_1 ended. Finally, pixel intensity curve 1306 shows the intensity of a pixel in the third segment.

Figure 13B in effect shows the combination of a portion of graph 1104 in Figure 11 and a portion of graph 1106 during a particular color subframe where the two graphs 1104 and 1106 have been merged. The graph 1310 shown in Figure 13B includes a pixel intensity curve 1318 for one pixel in the first segment and pixel intensity curve 1320 for a pixel in the second segment each of which have been loaded during their respective pixel loading times 1314 and 1316 onto their respective pixel electrodes. The illumination time is shown as being continuous illumination 1312. Note that in this embodiment of Figure 13B, the loading time t_1 equals the loading time t_2, and the liquid crystal switching time is T frame-t_1. T frame is shown in bold. Illuminating the display through both liquid crystal trajectories guarantees both segments will have the same brightness and the same behavior under temperature change.

Figure 13C illustrates an embodiment employing control electrode segments where the loading time has been slowed such that t_1 and t_2 become longer. The slowest possible data rate is achieved when $t_1=t_2=$tframe/2. This is illustrated in Figure 13C. This example results in the trajectories (relaxation of the crystals toward their final light altering state) of the liquid crystal on the top and bottom halves of the array being completely separate in time. Flood illumination for the time Tframe can be used as before. It may, however, be advantageous to pulse illuminate close to the ends of the trajectory. This will maximize the perceived contrast by only illuminating the brightest part of the curve for the bright pixels. Depending on the properties of the illuminator, it may be that the brightness of the illuminator is also increased, too. This slowest addressing scheme can be thought of as viewing the bottom half of the image while the top

half is being loaded, and then viewing the top half of the image while the bottom half is being loaded.

A scheme using pulse illumination with two pulses for each subframe in a time sequential system is shown in Figure 14 where there is one pulse near the end of the display for the first segment and one pulse near the end of the display for the second segment. This scheme 1401 shown in Figure 14 shows the trajectory of liquid crystals for one pixel 1404 after loading that pixel during time 1402 and also shows the trajectory of the liquid crystal for pixel 1410 after loading that pixel sometime during the time t_2 (shown as time 1408). The illumination pulses are not continuous and are separated by darkness.

Figure 15 shows an example where more than two pulses per color subframe can be used. In this example shown in Figure 15, t_1 and t_2 are shorter than the example shown in Figure 14. For example, t_1 1502 may equal t_2 1506 as in the case of the embodiment shown in Figure 11. Consequently, the liquid crystal material is allowed to progress up its switching curve for a longer time before it must be reset by the segmented control electrode. Pulse illumination (depending on the properties of the illuminator) may again be advantageous as compared to continuous illumination by sampling, on average, a better part of the liquid crystal switching dynamic. Positioning and time of the pulses is shown as follows. The rightmost pulse 1516 is positioned to illuminate the brightest part of the curve 1510 corresponding to the bottom segment. To maintain symmetry between both parts of the image, the corresponding part of the curve 1504 for the top part of the array is also illuminated with pulse 1514. Because, in this discussion, we are assuming flood illumination, that pulse also illuminates the liquid crystal on the bottom half of the array before it has reached its optimum state. Again, to maintain symmetry, we need to illuminate that corresponding part of the trajectory of the liquid crystal on the top half of the array represented by curve 1504. This determines the time of the earlier pulse 1512. Finally, to complete the symmetry, the pulse 1506 is also used. Now both curves 1504 and 1510 are illuminated identically, which in this example took four pulses. The number of pulses will depend on the timing of the liquid crystal trajectories. Note that in both cases the lowest contrast part of the curves is not illuminated.

It should be noted that a typical embodiment would employ control electrodes where the segments of the control electrodes are completely

disconnected electrically from each other. In an alternative embodiment, the control electrode segments may be coupled by a high resistance. For example, in the case of a cover glass electrode, the manufacturing process of the cover glass electrode may at first produce a common electrode having one segment which is then used to create two segments by etching or otherwise creating a separation between the two segments; however, this separation may not be complete and rather be a high-resistance connection between the two segments. It should also be noted that a spatial color system may use multiple control electrode segments provided by the invention. That is, rather than using time sequential color, an aspect of the invention uses a spatial color (having 3 different color subpixels, and the corresponding structure, for each pixel) system with multiple segments defined by multiple control electrode segments.

An advantage of most embodiments of the present invention is that simple pixel circuits can be made to update their optical outputs simultaneously, even if the pixel electrodes cannot be updated simultaneously. An example of such a pixel circuit is shown in Figure 6A which uses a signal transistor to load data onto a capacitor. The capacitance is usually formed between the pixel electrode and the control electrode which is often a common cover glass electrode, plus extra capacitance which can be obtained in a number of different ways, such as between the pixel electrode and a neighboring row select wire. This is illustrated in Figure 16A by the other capacitances 1604. The methods by which the other capacitances are formed depends on the details of the construction of the pixel array. For example, if the pixel array is formed on a single crystal silicon substrate or chip in a commercial CMOS fabrication process, there are typically several interconnect layers available which may be metal or polysilicon. These layers can be arranged during the design of the pixel array to provide extra capacitance which is advantageous in order to prevent decay of the image. Another way in which extra capacitance can be formed in this type of fabrication process is to define a region of thin oxide between the conductive plate (usually polycrystalline silicon) and the substrate material which may be doped. This thin oxide capacitor has a higher capacitance per unit area than the other capacitors which can be arranged. In this manner, the simple pixel circuits such as that shown in Figure 16A use capacitive storage to hold the electrode voltage on the pixel electrode until it is refreshed. Part of that capacitance is between the pixel electrode and the common electrode.

A consequence of this is that when the common electrode voltage is changed, after the pixels have been loaded with data, to release the liquid crystal from the dark state described above, the capacitive coupling between the common electrode and the pixel electrode may cause a change in the pixel electrode voltage which may require some compensation. This change is shown in Figure 16C which illustrates the common electrode voltage waveform 1619 having the reset portion 1619a and the release portions 1619b and four different pixel electrode voltages 1621a-1621d during the same time. Note that at the release point 1625, the pixel electrode voltages have changed as a result of the change in common electrode voltage.

The magnitude of the change in the pixel electrode voltage is determined by the magnitude of the change in common electrode voltage and the ratio of the capacitors shown in Figure 16A, including capacitors 1604 and the capacitance to the common electrode. It is not necessarily seriously detrimental for the pixel electrodes to exhibit some coupling to the common electrode (or a segmented electrode if a segment electrode is used). If all the pixels have the same capacitive coupling to the cover glass electrode, and the same extra capacitance, then they will all exhibit the same voltage shift which doesn't cause a loss of uniformity. This coupling does lead to the dilution of the effect of the control electrode modulation scheme of the present invention, leading to a requirement for it to be swung through a greater voltage range. Another possible problem involves a situation where the pixel array is fabricated in a single crystal silicon CMOS process and if the pixels are addressed by a single in-channel transistor then the electrode is isolated by the reversed bias PN junction at the FET terminal connected to the pixel electrode. If the voltage on the pixel electrode was pulled sufficiently low to cause this junction to become forward biased then charge would flow to clamp the voltage of the pixels. This would limit the useful voltage range that could be used on the pixel electrodes.

One approach to this issue is to arrange for extra capacitances which are shown in Figure 16A to be sufficiently large compared to the capacitance between the pixel electrode and the common electrode. If enough capacitance can be made available this method can allow the voltage movement of the electrode to be kept small enough to avoid detrimental effects. Another approach is to use a pixel circuit which has a buffer driving the pixel electrode. This is shown, for example, in Figure 6D. Another approach is to explicitly arrange for one of the extra

capacitors shown in Figure 16A to be connected to a signal which can be switched in opposition to the common electrode or control electrode. This extra electrode may be considered a compensation electrode which receives a compensation signal. If the pixel array is implemented in the CMOS process, the data wire could be first level metal, and the gate wire could be a second level metal, and the pixel electrode could be a third level metal. This is shown in Figure 16B where the pixel electrode 1632 is disposed over the compensation electrode 1630 which is disposed over the data wire in metal 1 which is 1634. The gate wire 1626 uses metal 2 and thus is at the same level as the compensation electrode 1630. The transistor 1605 of Figure 16A is shown as having a gate 1620, a source 1622, and a drain 1624; it will be appreciated that the source 1622 and the drain 1624 are in the substrate. There are many layer combinations which are available to construct extra capacitance and Figure 16B provides one example. It will be appreciated that the compensation electrode 1630 will be coupled to a driver circuit which drives a compensating electrode voltage 1627 in opposition to the common electrode voltage waveform 1619 shown in Figure 16D. As also shown in Figure 16D, the effect of the compensating electrode voltage is to maintain the pixel electrode voltage approximately unaffected by the common electrode voltage transition. The area of the overlap between the gate wire 1626 and the pixel electrode 1632 may be chosen so that the product of the capacitance between the pixel electrode and the common electrode, with the voltage swung by the common electrode, is approximately equal to the product of the capacitance between the pixel electrode and the compensation electrode, and the voltage that this wire was swung through in opposition to the common electrode transition. It will be appreciated that if the control electrode which in one embodiment is a common electrode is in fact segmented, then the compensating electrode 1630 should be segmented on the display as well in a corresponding manner.

In another aspect of the present invention, the compensating electrode may be used as a level shifting control in order to reset the liquid crystal material to a state in which display data is not visible as described above. That is, rather than using a cover glass electrode which may be a common electrode or a plurality of segments of electrodes, the electrodes similar to that electrode 1630 of Figure 16B may be used to modulate the liquid crystal layer in a fashion to reset and to release it as shown in Figure 2C above. In this manner, the segmentation of the control

electrode for providing resetting and releasing of the liquid crystal layer according to the present invention becomes easier as it is done on the same substrate which includes the pixel electrodes rather than attempting to create segments in a common cover glass electrode. The pixel circuit shown in Figure 16B may be used to provide such a control electrode such as electrode 1630 which would receive similar control signals as the cover glass electrode described above.

One example of using a control electrode in the same substrate as the pixel electrodes (such as electrode 1630) is shown in Figure 16E. The example of Figure 16E assumes that the cover glass electrode is fixed at $V_{dd}/2$ (shown as signal 1651) and that the pixel electrodes can be set to any value between zero volts and V_{dd}. The control electrodes in the substrate with the pixel electrodes are switched between one state (at V_{dd}) and another state (at V=0) as shown by waveform 1653. During one state of the control electrodes in one frame, the display data is substantially not viewable as shown by the waveforms 1655. During the released state of the control electrode, the display data is viewable as shown by the rising trajectories in the waveforms 1655. The pixel values are loaded onto the pixel electrodes during the reset state of the control electrodes while the display is held to a dark state, and upon the entry to the release state, the capacitive coupling between the control electrodes and the pixel electrodes simultaneously shifts the voltage of these pixel electrodes as shown by the pixel electrode waveforms 1657. The scheme of Figure 16E uses time sequential color with three color subframes per frame and uses DC balancing between frames. Thus the reset state by the control electrodes in one frame 1659 occurs when the control electrodes are held at V_{dd} and the released state in frame 1659 occurs when the control electrodes are held at zero volts. Similarly, the reset state by the control electrodes in frame 1661 occurs when the control electrodes are held at zero volts and the released state occurs when the control electrodes are at V_{dd}.

Some liquid crystal display systems utilize a frame sequential DC balancing scheme in which the liquid crystal is DC balanced by writing data such that the sequence of images is alternately written of positive and then negative polarity. Given that any pixel electrode of the display substrate can be driven to a voltage in the range between V_{max} and V_{min}, if the common electrode is fixed at a voltage halfway between V_{max} and V_{min}, then the maximum DC balanced signal that can

be applied to the liquid crystal alternates between $+(V_{max}-V_{min})/2$ and $-(V_{max}-V_{min})/2$ in sequential frames, resulting in an RMS voltage of $(V_{max}-V_{min})/2$.

Several different forms of common electrode voltage modulation may be performed according to various embodiments of the present invention. With reference to Figure 17, according to an embodiment of the invention which utilizes a pixel buffer with the pixel electrode (on the same substrate, e.g. as shown in Figure 6D), voltage of common electrode 26 of display system 12 may be modulated between V_{max} and V_{min}. By driving common electrode 26 to V_{min} during the "positive" frame of such an electrical addressing scheme and to V_{max} during the "negative" frame, the voltage of the maximum DC balanced RMS signal appearing across the electro-optic layer is doubled from $(V_{max}-V_{min})/2$ to $V_{max}-V_{min}$ (RMS).

For example, during the "positive" frame, a pixel which is to be driven to a bright state is assumed to require a high voltage at the pixel electrode. (Note, however, that the opposite situation could also hold true, i.e. a high voltage of common electrode 26 could drive a pixel to the dark state, depending on the configuration of electro-optic layer or liquid crystal used.) According to the present invention, the common electrode may be driven to V_{min} during the "positive" frame. Therefore, the voltage that can be presented across electro-optic layer 22 ranges from $V_{min}-V_{min}$ to $V_{max}-V_{min}$, and is identical to the voltage range available at a pixel electrode 28.

In the "negative" frame the common electrode is driven to V_{max}, and a bright state is achieved by driving the pixel electrode to a low voltage so as to maximize the voltage across electro-optic layer 22. In this case the voltage that can be presented across electro-optic layer 22 ranges from $V_{max}-V_{max}$ to $V_{min}-V_{max}$. In the example shown in Figure 17 the pixel electrode is driven so that the voltage across the electro-optic layer is about 2/3 of the maximum available voltage. One subclass of display systems allows the pixel electrodes to be simultaneously updated with data corresponding to a new image. Such display systems are described in U.S. patent application serial number 08/505,654, the contents of which are incorporated herein by reference and will be referred to as frame (subframe) sequential display devices. Since the pixels are simultaneously updated for this type of display, the pixel electrodes do not have to be driven to voltages other than their data voltages (and their inverses for DC balance) when the

common electrode is modulated, which simplifies the drive circuitry, according to one embodiment of the invention.

This is different from a row-at-a-time update of the pixel electrode. One way this can be done in active matrix display is to drive the reference plates of the pixel data storage capacitors through a voltage sequence which mimics the common electrode voltage modulation. This could be done by driving all the row gate wires synchronously with the common electrode, at the cost of increased complexity and power dissipation. See for example U.S. Patent No. 5,561,422, the contents of which are incorporated herein by reference.

According to another embodiment of the invention common electrode 26 is driven to voltages other than V_{min} and V_{max} in the phase relationship described above. For example, as shown in Figure 18, common electrode 26 could be driven to a voltage less than V_{min} (e.g. to V_{min}-V_{offset}) during the "positive" frame, and to a voltage greater than V_{max} (e.g. to V_{max}+V_{offest}) during the "negative" frame. The result of such a scheme is that the voltage range that can be applied to electro-optic layer 22 is now shifted to V_{offset} as the minimum addressing voltage, and to V_{offset} + (V_{max}-V_{min}) as the maximum addressing voltage.

The embodiment of the present invention exemplified by the schematic representation of Figure 18 could find applications in situations where, for example, the liquid crystal electro-optic effect has a minimum threshold voltage level below which no optical effect occurs. By choosing V_{offset} in such a way as to take up some, or all, of this offset the full range of voltage available at the pixel electrode is available for electro-optic modulation.

The present application hereby incorporates herein by reference the parent U.S. patent application filed on December 19, 1996, serial number 08/770,233.

Various alternative embodiments of the present invention employ a control device which is coupled to at least one of the pixel electrodes in order to apply a reference voltage to the pixel electrode before the display system displays the next frame or subframe. Examples of these embodiments will be described by referring to Figures 19, 20, and 21.

Figure 19 is a flowchart which illustrates one embodiment of the present invention in which a reference voltage is applied to pixel electrodes. In this embodiment, the cover glass voltage is set in step 1901 so as to alter the state of

the liquid crystal material so that old pixel data is substantially not viewable. In a typical embodiment, the display frame will be driven momentarily dark even if pixel data is still stored on the pixel electrodes. Then in step 1903, a control device, or several control devices, apply a reference voltage to all pixel electrodes. In the case of a display system according to the present invention which uses a segmented cover glass such as that shown in Figure 10A, then only the pixel electrodes within a particular segment will receive the reference voltage. It will be appreciated that step 1903 may occur just before, or simultaneously with step 1901 as well as just after step 1901 as shown in Figure 19. In step 1905, the control device or devices stop applying the reference voltage to all pixel electrodes. This allows the loading of data for the next frame or subframe in step 1907. If the display system employs row by row loading of pixel data, then the loading occurs in this manner while the cover glass voltage is maintained to keep pixel data substantially not viewable. Alternatively, the loading of the data may occur by an entire frame at a time if the next frame is buffered in circuit such as the example shown in Figure 6D. In step 1909, the cover glass voltage is released to allow the display of data for the next frame which may be a full color frame or a color subframe. This process is repeated for the next frame or subframe.

The reference voltage applied to the pixel electrodes may be ground or some other reference voltage. This reference voltage may alternate over time in order to get a DC balanced signal over time on the pixel electrodes (ignoring the pixel data values).

This alternative embodiment may be employed with time sequential color wherein each frame is actually a color subframe or it may be employed in display systems which have three different color subpixels for each pixel. Moreover, this alternative may be employed with a reset control voltage which has the same value throughout the period in which the display data is not viewable or it may be employed with a cover glass control voltage which has a pulse at the beginning of the time in which the display data is substantially not viewable. Moreover, it will be appreciated that the method shown in Figure 19 may be practiced in an alternative sequence in which steps 1909 and 1905 are done together in the case where the next frame of image data is buffered. In this case, the resetting of the display caused by modulating the cover glass voltage and the application of the reference voltage would occur substantially concurrently and then the cover glass

voltage would be released and the reference voltage would be released while new data is loaded from the buffer.

Figure 20 shows several waveforms over time. These waveforms may be employed with alternative embodiments of the present invention in which the pixel electrodes are set to a reference voltage. Waveform 2001 represents the voltage on a cover glass electrode or other control electrode such as a segmented cover glass or the compensating electrodes described herein. Waveform 2003 shows the clamp control voltage or the clamp in voltage ($V_{clamp\ in}$), which voltage is supplied to a control device to cause the control device to apply a first reference voltage to pixel electrodes in the display system. Waveforms 2005 and 2007 represent the voltages applied to exemplary row or word lines X and Y on an integrated circuit which forms a part of the display system of the present invention. Waveform 2009 shows the times when an image can be displayed over time as a result of the cover glass voltage shown by waveform 2001 and the loading of pixel data onto the pixel electrodes.

At time 2021, the cover glass voltage is driven to a high voltage which may be considered a hard reset; this state of the cover glass exists during the period between times 2021 and 2023. During this time, the clamp control voltage is also driven high as shown by waveform 2003 and both row lines x and y are driven high while the data columns receive a first reference voltage. The high clamp control voltage causes a first reference voltage to be applied to the pixel electrodes. Typically this will mean that the pixel electrodes will be driven to ground and that all pixel electrodes will have the same voltage state. It will be appreciated that the clamp control voltage may be applied during only a portion of the time between times 2021 and 2023. Moreover, the clamp control voltage may be applied after the hard reset period (after time 2023) although this tends to reduce the actual display time.

At time 2023, the hard reset voltage is released as shown by waveform 2001 and now the cover glass is set at a lower voltage which exists during the time between times 2023 and 2029. During this time, pixel data is loaded onto the pixel electrodes as shown by the waveforms 2005 and 2007 which represent the write controls to the word lines on the integrated circuit which form a part of the display system of the present invention. The activation of these rows is shown at times 2025 and 2027. Also during this time, the clamp control voltage is reduced back

to its non-asserted level such that the pixel data may now be loaded onto the pixel electrodes. At time 2029, the "hold" voltage which has been applied to the cover glass is released and now the cover glass voltage falls as shown by waveform 2001. At this time, display data is now capable of being viewed as shown by the portion 2009a of the waveform 2009. Thus the actual display time for this frame (or subframe) is between times 2029 and 2031.

At step 2031, the cover glass voltage is again changed such that the display data displayed during portion 2009a is no longer viewable. During the time of the "hard reset" of the display which occurs during times 2031 and 2033, the clamp control voltage is again asserted as shown by the waveform 2003 and the row lines x and y are driven high which again causes the pixel electrodes to be driven to a reference voltage. At time 2033, the clamp control voltage is changed to allow the pixel electrodes to be loaded at times such as 2035 and 2037. Also at time 2033, the voltage on the cover glass is changed as shown by the waveform 2001 at time 2033. Then at time 2039, the voltage on the cover glass is changed again to allow the display data loaded between times 2033 and 2039 to be displayed during portion 2009b of the waveform 2009. This process continually repeats itself during a display of data in the display system of this alternative embodiment of the present invention.

It should also be understood that certain liquid crystal materials can be reset by application of an alternating current signal. This can be accomplished by driving the cover glass voltage (V_{CG}) signal (represented by waveform 2001 in the example of Figure 20) with an oscillating signal during the duration of the "clamping" portion of the reference signal ($V_{clamp\ in}$, such as between the times 2021 and 2023 as shown in Figure 20. In this example, it may also be advantageous to also drive the pixel reference voltage ($V_{clamp\ in}$, shown by waveform 2003) with an oscillating signal during the "clamping" portion of this signal (e.g. between times 2021 and 2023), where this oscillating signal is out of phase with the V_{CG} oscillating signal during the same "clamping" times. This has the effect of reducing the supply voltages required to perform the reset of the display which occurs at times 2021 and 2031 as shown in Figure 20.

Figure 21 shows an example of an array of pixel electrodes disposed on a substrate of an integrated circuit which forms part of the present invention. It will be appreciated that this circuit is only one of many possible examples which may

be implemented according to this alternative of the present invention. The integrated circuit 2101 includes two column electrodes or lines 2103 and 2105 and two row electrodes or lines 2107 and 2109. The intersection of each column and row forms a pixel cell which includes a pixel electrode, such as pixel electrodes 2127b, 2128b, 2129b, and 2130b which are controlled by field effect transistors (FET) 2127a, 2128a, 2129a, and 2130a respectively. The integrated circuit 2101 also includes a row select driver 2111 which controls the driving of the various row electrodes to enable loading of new pixel data onto each row of pixel electrodes. It will be appreciated that the row select driver 2111 may be a conventional row select driver employed with active matrix reflective liquid crystal display devices such as liquid crystal on silicon display devices described above. It will also be appreciated that each pixel cell may be a conventional pixel cell as employed in active matrix reflective display liquid crystal on silicon display devices.

Each column electrode or line is coupled respectively to a column driver. Thus, column 2103 is coupled to the column driver 2115, and column 2105 is coupled to the column driver 2117. Each column driver has an input to receive data which is to be driven to a pixel electrode at the intersection of the currently enabled row in that particular column. It will be appreciated that the column driver coupled to each column may be a conventional column driver as used with active matrix reflective liquid crystal on silicon display systems. The input to each column driver is from an output of a multiplexer. Two such multiplexers are shown in Figure 21 as multiplexers 2119 and 2121. Each multiplexer receives an input from a clamp reference voltage 2125 which is selectively coupled to the pixel electrodes to provide the clamp reference voltage 2125 through the multiplexers 2119 and 2121. The clamp in voltage control also controls the selection of the output from the multiplexers 2119 and 2121 such that during the assertion of the clamp control voltage (e.g. between times 2021 and 2023 as shown in Figure 20) the multiplexer selects for output the clamp reference voltage provided by the clamp reference voltage generator 2125. During other modes of operation, the clamp in voltage is not asserted and the multiplexer selects for input to its respective column driver the column data input for that particular column as shown in Figure 21. The clamp in voltage control (or clamp control voltage) is also applied to the gate of the field effect transistors 2131 and 2133 which cause each

row to be pulled high to thereby turn on each field effect transistor within a pixel cell. Thus, when the clamp in voltage is asserted (e.g. between times 2031 and 2033 shown in Figure 20) the field effect transistors in each pixel cell will conduct the clamp reference voltage from the clamp reference voltage source 2125 to its respective pixel electrodes. In one embodiment, the clamp reference voltage 2125 may be merely ground such that all pixel electrodes are discharged to ground during the portion of time in which the clamp in voltage is asserted. This portion of time will typically be before the loading of the next pixel data such that all pixel electrodes consistently have the same voltage values. Other values for the clamp reference voltage may be utilized, and this clamp reference voltage may be varied over time.

It will be appreciated that the integrated circuit 2101 may be employed with a segmented cover glass by having two banks (or more banks) of rows each of which receives a separate clamp control voltage in order to select each bank to drive the pixel electrodes within each bank to a reference voltage.

Figure 22 shows another example of an array of pixel electrodes disposed on a substrate of an integrated circuit (IC) which forms part of the present invention. The IC 2102 of Figure 22 is similar to the IC 2101 of Figure 21 and contains many of the same components. The outputs from the row selector 2111 are provided to a plurality of OR gates, each of which also receives a clamp in voltage control signal (e.g. the waveform 2003 of $V_{clamp\ in}$ shown in Figure 20) which is asserted high to pull the row lines high when the clamp reference voltage is applied to the pixel electrodes in the rows. Figure 22 shows two OR gates 2151 and 2152, each receiving one input from the row selector 2111 and one input from the clamp in voltage control signal. The output of each gate is coupled to one row line.

It will also be appreciated that certain embodiments of the present invention which utilize a pixel buffer within each pixel cell may employ the foregoing technique of setting the pixel electrodes to a reference voltage value. Figure 6D and the accompanying description provide such an example where the pixel electrode voltage is discharged prior to loading new pixel data onto the pixel electrode.

It will be appreciated that typical embodiments of the present invention require an electro-optic material, such as a liquid crystal material, to provide fast

switching times. This is particularly true of a display system which uses time sequential color by displaying color subframes in rapid sequence. Consequently, the present invention preferably does not employ liquid crystal materials which have metastable states which last for many seconds.

It may, in certain implementations of the invention, be advantageous to shift the reference voltage (e.g. V_{CG} which drives the cover glass electrode) by a small offset voltage for the entire waveform of the reference voltage. This shift would then maintain a slight DC voltage over time across the electro-optic layer; thus, rather than having a DC balanced signal over time across this layer (e.g. across the liquid crystal) which is balanced at V = 0 (a direct current measurement), the DC voltage across the layer over time is "balanced" at V = offset voltage. The advantage of this is that it can be used to remove asymmetry in the behavior of certain liquid crystals and make a display with less flicker.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the pending claims. The specification and drawings are, accordingly, to be regarded in an illustrative sense rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A display system comprising:

a first substrate having a first plurality of pixel electrodes for receiving a first plurality of pixel data values representing a first image to be displayed;

an electro-optic layer operatively coupled to said pixel electrodes;

an electrode operatively coupled to said electro-optic layer, said display system displaying said first image and then applying a first control voltage to said electrode to alter a state of said electro-optic layer such that said first image is substantially not displayed and then said display system displaying a second image represented by a second plurality of pixel data values after said electrode receives a second control voltage;

a control device coupled to at least one of said pixel electrodes, said control device applying a first reference voltage to at least one of said pixel electrodes before said display system displays said second image.

2. A display system as in claim 1 wherein said control device is coupled to said first plurality of pixel electrodes and applies said first reference voltage to said first plurality of pixel electrodes.

3. A display system as in claim 1 wherein said control device comprises a multiplexer.

4. A display system as in claim 1 wherein said first reference voltage is applied to said one of said pixel electrodes during at least a portion of a time that said first image is substantially not displayed.

5. A display system as in claim 1 further comprising:

a first row electrode coupled to a first row of pixel electrodes, said first row of pixel electrodes being a subset of said first plurality of pixel electrodes;

a plurality of column drivers, each of which is coupled to a respective pixel electrode of said first row of pixel electrodes, and wherein said control device is coupled to at least one of said column drivers.

6. A display system as in claim 5 wherein said electro-optic layer comprises a liquid crystal material and wherein said control device is coupled to each of said plurality of column drivers.

7. A display system as in claim 6 wherein said first reference voltage is applied to each pixel electrode of said first row of pixel electrodes during at least a portion of a time that said first image is substantially not displayed.

8. A display system as in claim 7 wherein said first image comprises a first color subframe and said second image comprises a second color subframe.

9. A display system as in claim 7 wherein said second plurality of pixel data values is applied to said first plurality of pixel electrodes after said first reference voltage is applied to said first plurality of pixel electrodes.

10. A display system as in claim 9 wherein said control device allows said plurality of column drivers to apply said second plurality of pixel data values to said first plurality of pixel electrodes after said first reference voltage is applied to said first plurality of pixel electrodes.

11. A display system as in claim 10 wherein said electrode provides a third control voltage after said first control voltage and before said step of applying said second control voltage, wherein said third control voltage holds said electro-optic layer in a first light altering state and said first control voltage rapidly places said electro-optic layer in said first light-altering state, and wherein said control device allows said plurality of column drivers to apply said second plurality of pixel data values to said first plurality of pixel electrodes while said third control voltage holds said electro-optic layer in said first light altering state.

12. A display system comprising:

a first substrate having a first plurality of pixel electrodes for receiving a first plurality of pixel data values representing a first portion of an image and having a second plurality of pixel electrodes for receiving a second plurality of pixel data values representing a second portion of said image;

an electro-optic layer having a first portion of said electro-optic layer operatively coupled to said first plurality of pixel electrodes and having a second portion of said electro-optic layer operatively coupled to said second plurality of pixel electrodes;

a first electrode coupled to a first electrode control driver and operatively coupled to said first portion of said electro-optic layer, said first electrode receiving a first control voltage to alter a state of said first portion of said electro-optic layer such that said first portion of said image is substantially not displayed;

a second electrode coupled to a second electrode control driver and operatively coupled to said second portion of said electro-optic layer, said second electrode receiving a second control voltage to alter a state of said second portion of said electro-optic layer such that said second portion of said image is substantially not displayed;

a first control device coupled to said first plurality of pixel electrodes, said first control device applying a first reference voltage to said first plurality of pixel electrodes during at least a portion of time when said first portion of said image is substantially not displayed;

a second control device coupled to said second plurality of pixel electrodes, said second control device applying said first reference voltage to said second plurality of pixel electrodes during at least a portion of time when said second portion of said image is substantially not displayed.

13. A display system as in claim 12 wherein a first electrode is a first portion of a cover glass and said second electrode is a second portion of said cover glass.

14. A display system as in claim 12 wherein said first plurality of pixel electrodes are coupled to a first plurality of row electrodes and said second plurality of pixel electrodes are coupled to a second plurality of row electrodes and said first control device is coupled to said first plurality of row electrodes and said second control device is coupled to said second plurality of row electrodes.

15. A display system as in claim 14 wherein said electro-optic layer comprises a liquid crystal material and wherein said liquid crystal has at least a first light altering state and a second light altering state and wherein said first and said second control voltages set said liquid crystal in said first light altering state such that light cannot pass through said display system and said first electrode control driver and said second electrode control driver respectively provide a third control voltage and a fourth control voltage which set said liquid crystal in said second light altering state such that light is capable of passing through said display system.

16. A method for operating a display system, said display system comprising a first substrate having a plurality of pixel electrodes, an electro-optic layer operatively coupled to said pixel electrodes, a control device coupled to at least one of said pixel electrodes and an electrode operatively coupled to said electro-optic layer, said method comprising:

applying a first plurality of pixel data values to said plurality of pixel electrodes such that a first pixel data represented by said first plurality of pixel data values is displayed;

applying a first control voltage to said electrode to alter a state of said electro-optic layer such that said first pixel data is substantially not displayed;

applying a first reference voltage to at least one of said pixel electrodes;

applying a second plurality of pixel data values to said plurality of pixel electrodes, said second plurality of pixel data values representing a second pixel data; and

displaying said second pixel data.

17. A method as in claim 16 wherein said first reference voltage is applied to said plurality of pixel electrodes before applying said second plurality of pixel data values and wherein said step of displaying said second pixel data comprises:

applying a second control voltage to said electrode to alter said state of said electro-optic layer such that said second pixel data is displayed, and

wherein a first image is represented by said first pixel data and a second image is represented by said second pixel data.

18. A method as in claim 17 wherein said first image comprises a first color subframe and said second image comprises a second color subframe.

19. A method as in claim 17 wherein said electro-optic layer comprises a liquid crystal material and wherein said liquid crystal has at least a first light altering state and a second light altering state and wherein said first control voltage sets said liquid crystal in said first light altering state such that light cannot pass through said display system.

20. A method as in claim 19 wherein said second control voltage sets said liquid crystal in said second light altering state such that light is capable of passing through said display system.

21. A method as in claim 17 further comprising:

applying a third control voltage to said electrode after applying said first control voltage and before said step of applying said second control voltage, wherein said third control voltage holds said electro-optic layer in a first light altering state and said first control voltage rapidly places said electro-optic layer in said first light altering state.

22. A method for operating a display system, said display system comprising a first substrate having a first plurality of pixel electrodes coupled to a first control device and a second plurality of pixel electrodes coupled to a second control device, an electro-optic layer operatively coupled to said first and said second

plurality of pixel electrodes, and a first electrode and a second electrode, said method comprising:

applying a first plurality of pixel data values to said first plurality of pixel electrodes, said first plurality of pixel data values representing a first portion of an image;

applying a first control voltage to said first electrode to alter a state of a first portion of said electro-optic layer such that said first portion of said image is not displayed;

applying a first reference voltage to at least one of said first plurality of pixel electrodes;

displaying said first portion of said image;

applying a second plurality of pixel data values to said second plurality of pixel electrodes, said second plurality of pixel data values representing a second portion of said image;

applying a second control voltage to said second electrode to alter a state of a second portion of said electro-optic layer such that said second portion of said image is not displayed;

applying said first reference voltage to at least one of said second plurality of pixel electrodes; and

displaying said second portion of said image.

23. A method as in claim 22 wherein said first electrode is a first portion of a cover glass electrode disposed on a second substrate and said second electrode is a second portion of said cover glass electrode, said first portion and said second portion of said cover glass electrode not being electrically coupled.

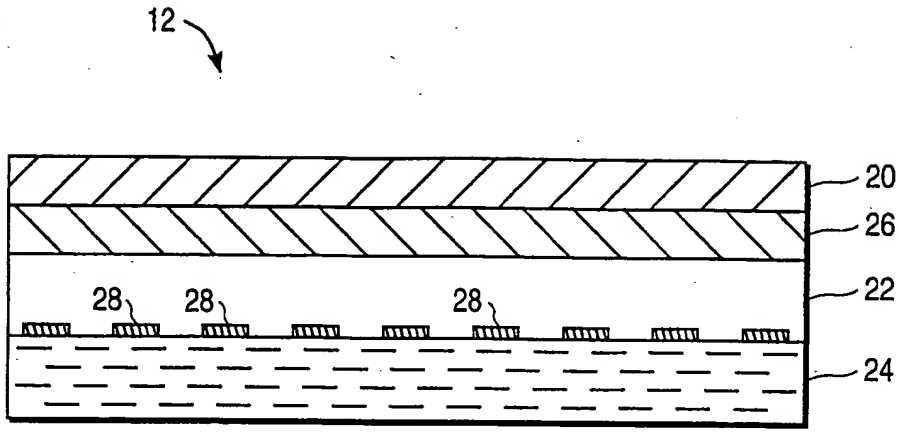


FIG. 1A

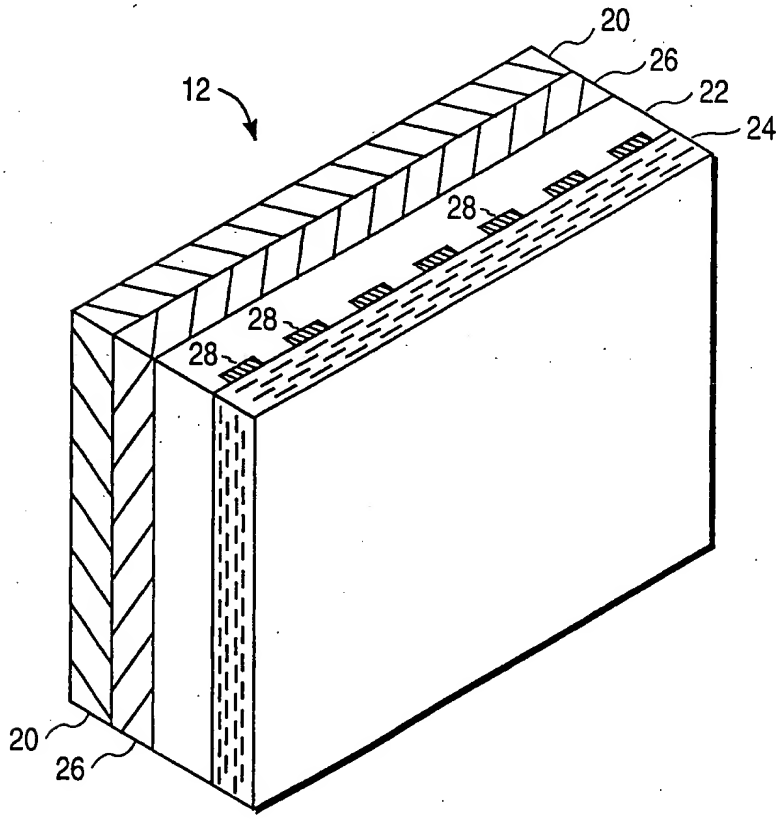


FIG. 1B

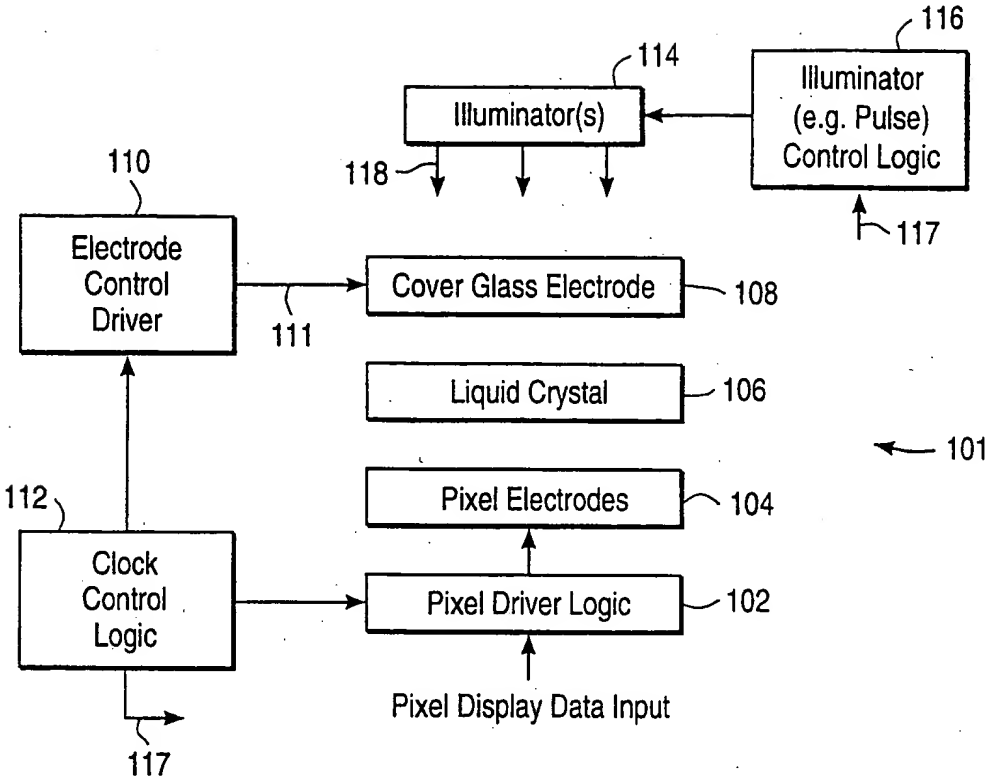
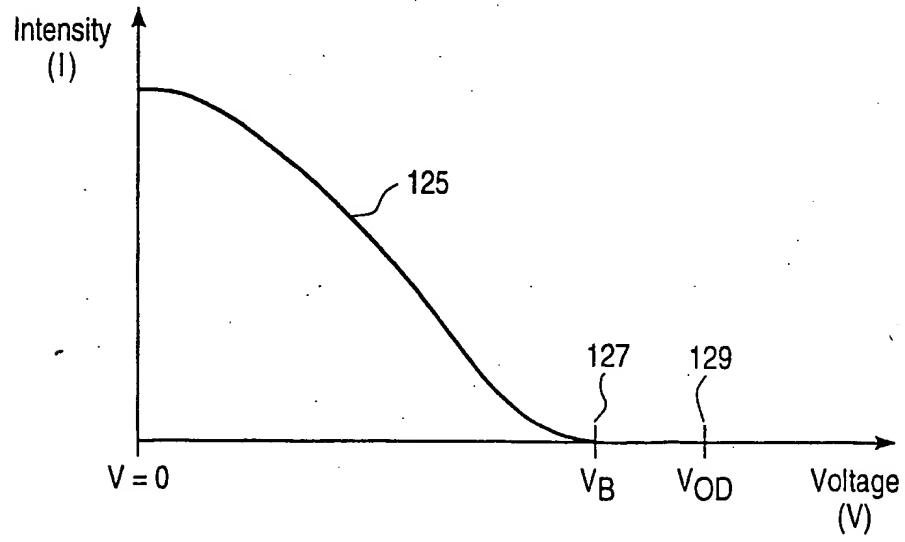


FIG. 2A



Electro-optic Curve for
Normally White Liquid Crystal

FIG. 2B

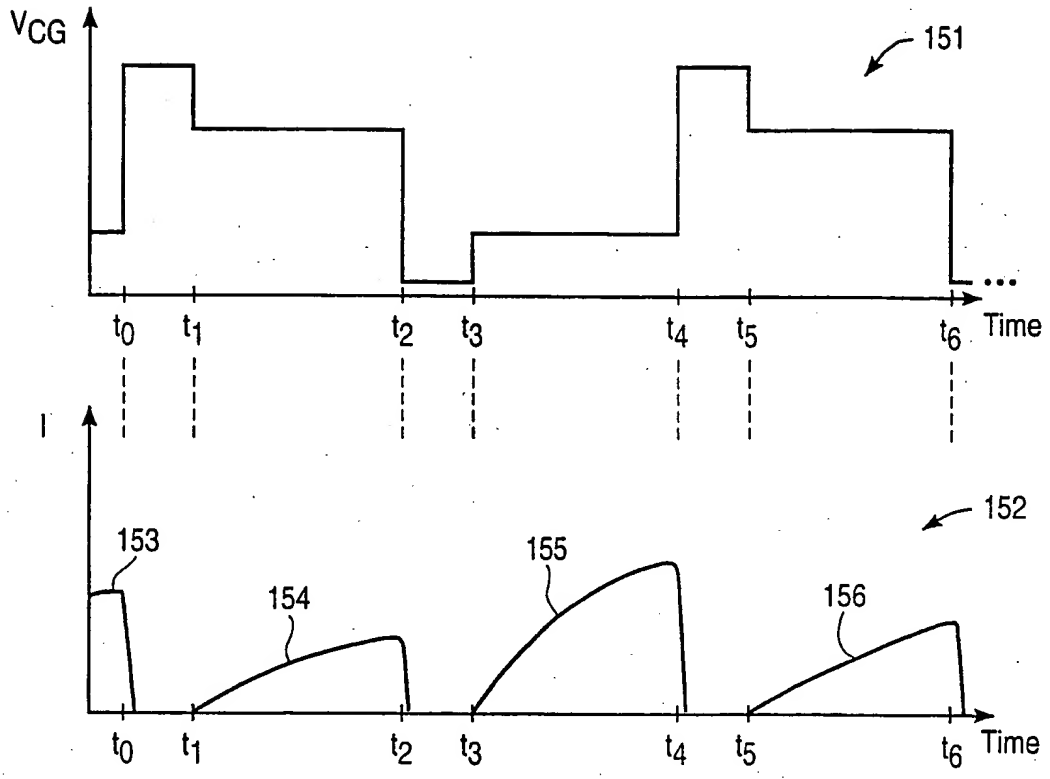

V_{CG}
151
t_0 t_1 t_2 t_3 t_4 t_5 t_6 Time
I
152
153
154
155
156
t_0 t_1 t_2 t_3 t_4 t_5 t_6 Time

FIG. 2C

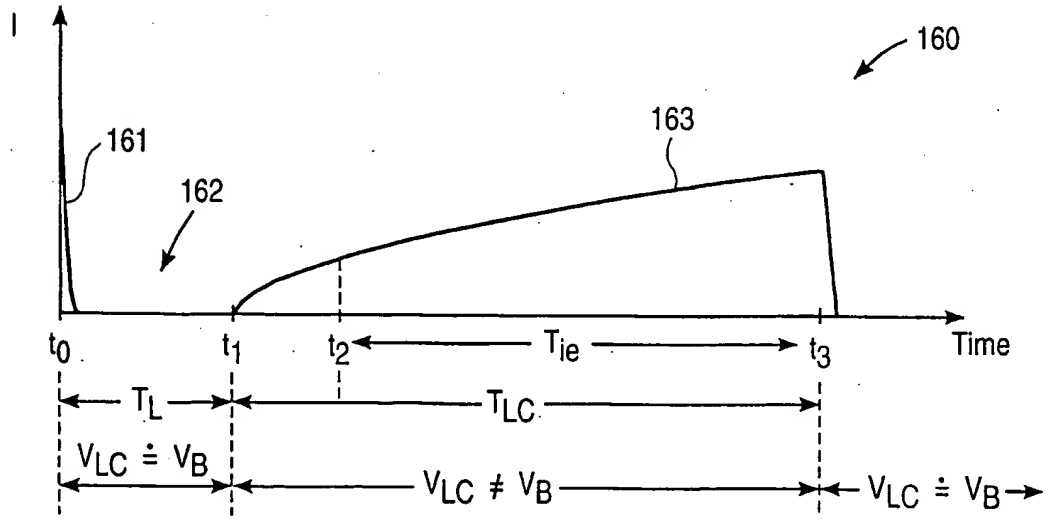

I
160
161
162
163
t_0 t_1 t_2 T_{ie} t_3 Time
T_L
T_{LC}
$V_{LC} \doteq V_B$
$V_{LC} \neq V_B$
$V_{LC} \doteq V_B$

FIG. 2D

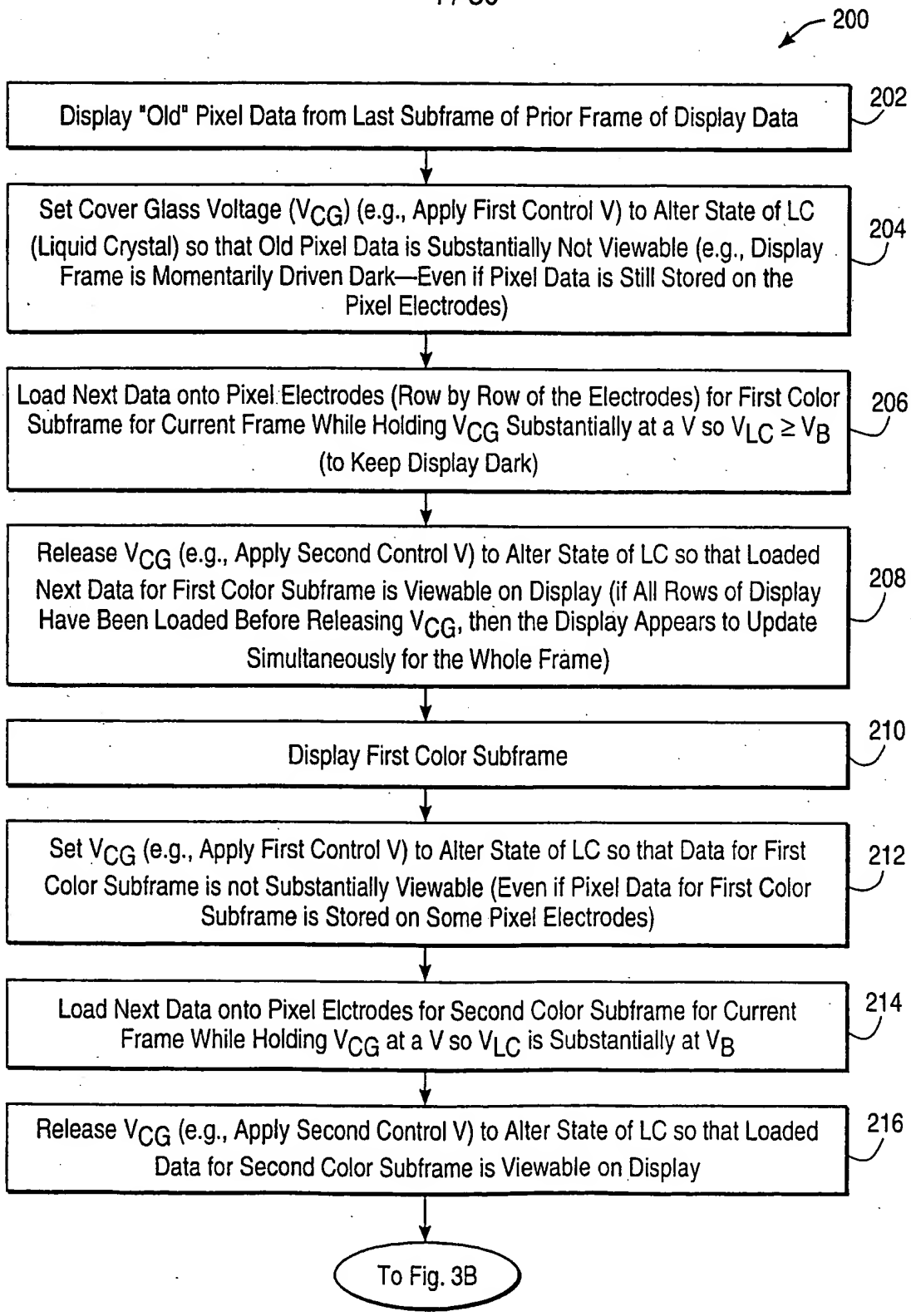

200
Display "Old" Pixel Data from Last Subframe of Prior Frame of Display Data
202
Set Cover Glass Voltage (V_{CG}) (e.g., Apply First Control V) to Alter State of LC (Liquid Crystal) so that Old Pixel Data is Substantially Not Viewable (e.g., Display Frame is Momentarily Driven Dark—Even if Pixel Data is Still Stored on the Pixel Electrodes)
204
Load Next Data onto Pixel Electrodes (Row by Row of the Electrodes) for First Color Subframe for Current Frame While Holding V_{CG} Substantially at a V so $V_{LC} \geq V_B$ (to Keep Display Dark)
206
Release V_{CG} (e.g., Apply Second Control V) to Alter State of LC so that Loaded Next Data for First Color Subframe is Viewable on Display (if All Rows of Display Have Been Loaded Before Releasing V_{CG}, then the Display Appears to Update Simultaneously for the Whole Frame)
208
Display First Color Subframe
210
Set V_{CG} (e.g., Apply First Control V) to Alter State of LC so that Data for First Color Subframe is not Substantially Viewable (Even if Pixel Data for First Color Subframe is Stored on Some Pixel Electrodes)
212
Load Next Data onto Pixel Elctrodes for Second Color Subframe for Current Frame While Holding V_{CG} at a V so V_{LC} is Substantially at V_B
214
Release V_{CG} (e.g., Apply Second Control V) to Alter State of LC so that Loaded Data for Second Color Subframe is Viewable on Display
216
To Fig. 3B

FIG. 3A

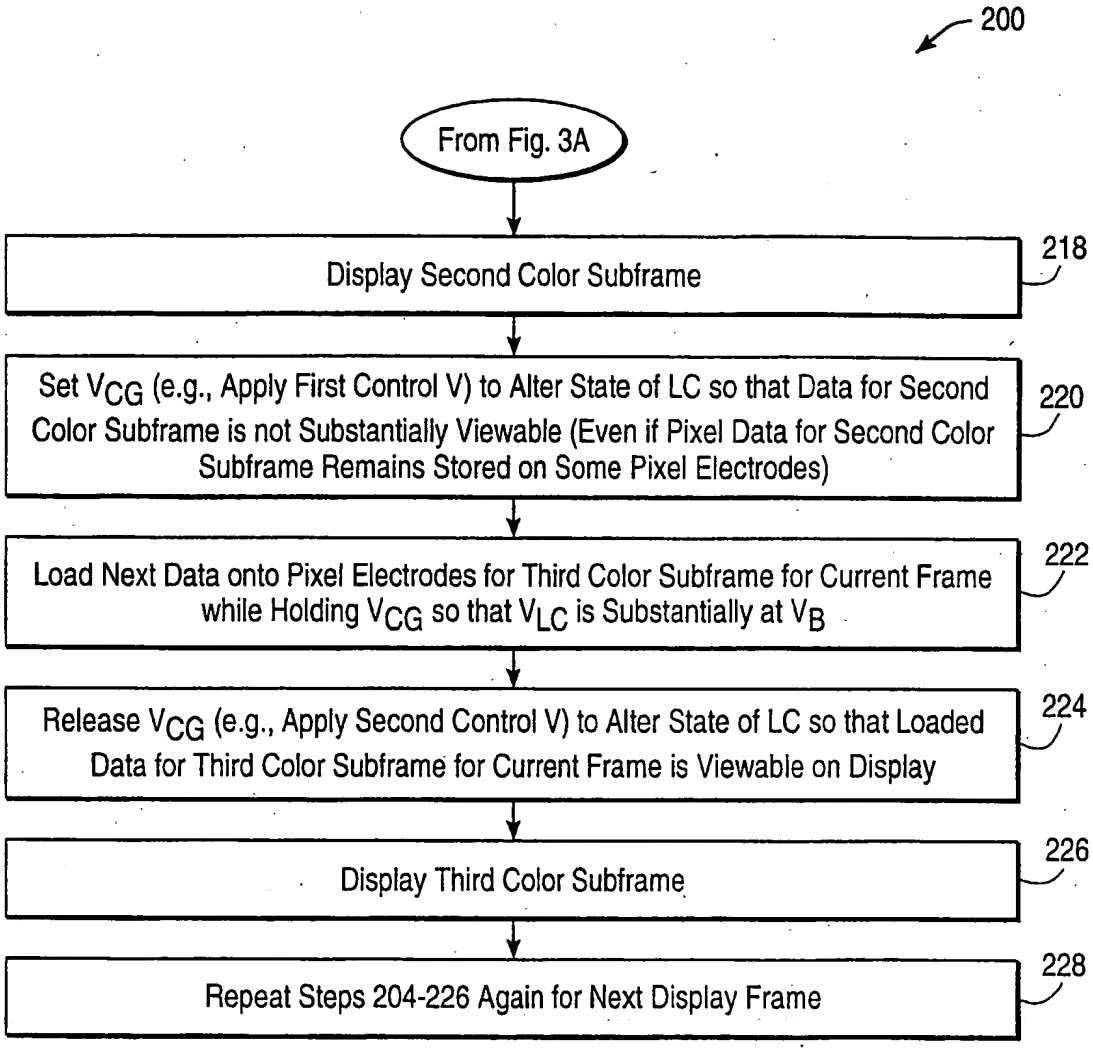

200
From Fig. 3A
Display Second Color Subframe
218
Set V_{CG} (e.g., Apply First Control V) to Alter State of LC so that Data for Second Color Subframe is not Substantially Viewable (Even if Pixel Data for Second Color Subframe Remains Stored on Some Pixel Electrodes)
220
Load Next Data onto Pixel Electrodes for Third Color Subframe for Current Frame while Holding V_{CG} so that V_{LC} is Substantially at V_B
222
Release V_{CG} (e.g., Apply Second Control V) to Alter State of LC so that Loaded Data for Third Color Subframe for Current Frame is Viewable on Display
224
Display Third Color Subframe
226
Repeat Steps 204-226 Again for Next Display Frame
228

FIG. 3B

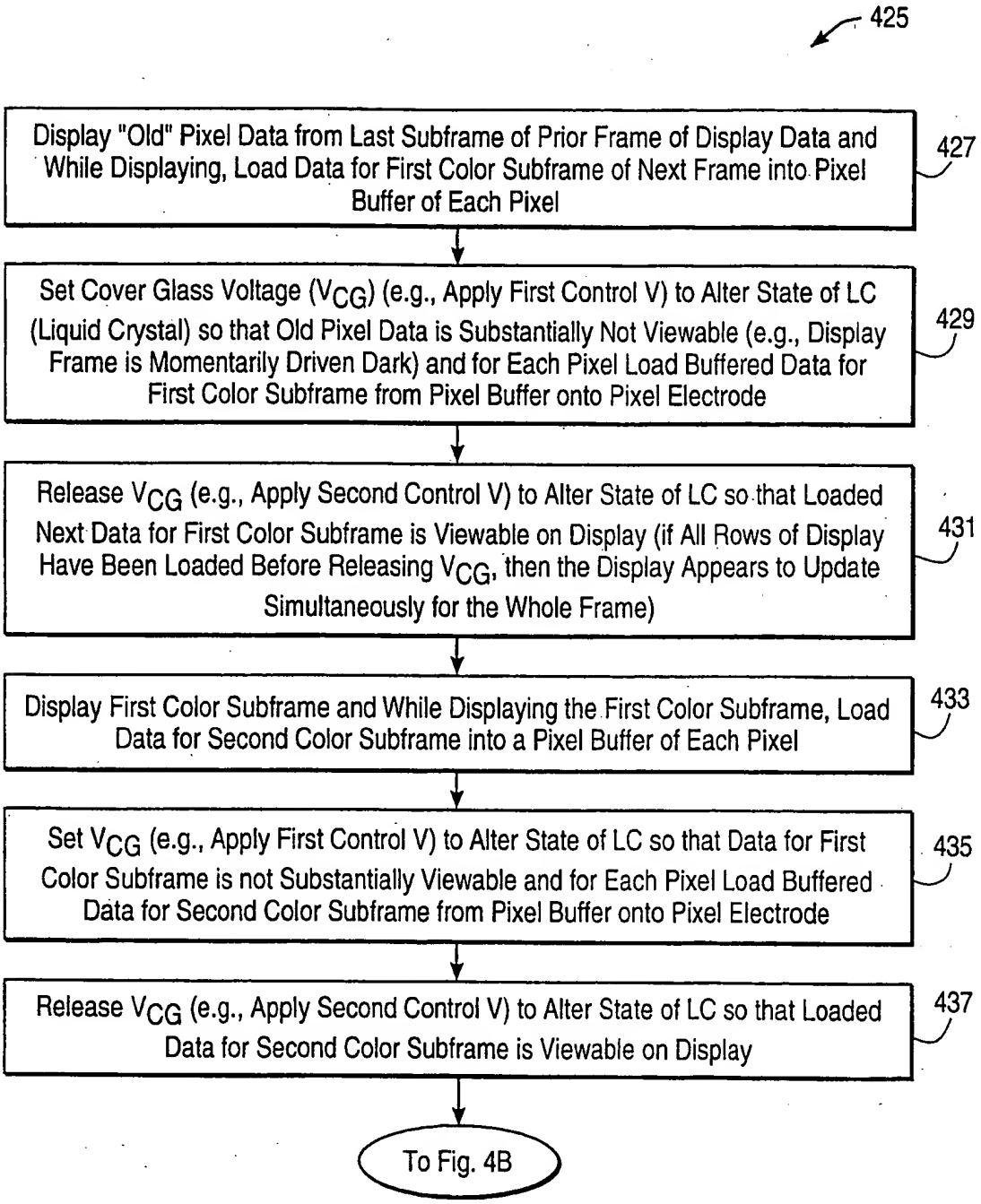

425
Display "Old" Pixel Data from Last Subframe of Prior Frame of Display Data and While Displaying, Load Data for First Color Subframe of Next Frame into Pixel Buffer of Each Pixel
427
Set Cover Glass Voltage (V_{CG}) (e.g., Apply First Control V) to Alter State of LC (Liquid Crystal) so that Old Pixel Data is Substantially Not Viewable (e.g., Display Frame is Momentarily Driven Dark) and for Each Pixel Load Buffered Data for First Color Subframe from Pixel Buffer onto Pixel Electrode
429
Release V_{CG} (e.g., Apply Second Control V) to Alter State of LC so that Loaded Next Data for First Color Subframe is Viewable on Display (if All Rows of Display Have Been Loaded Before Releasing V_{CG}, then the Display Appears to Update Simultaneously for the Whole Frame)
431
Display First Color Subframe and While Displaying the First Color Subframe, Load Data for Second Color Subframe into a Pixel Buffer of Each Pixel
433
Set V_{CG} (e.g., Apply First Control V) to Alter State of LC so that Data for First Color Subframe is not Substantially Viewable and for Each Pixel Load Buffered Data for Second Color Subframe from Pixel Buffer onto Pixel Electrode
435
Release V_{CG} (e.g., Apply Second Control V) to Alter State of LC so that Loaded Data for Second Color Subframe is Viewable on Display
437
To Fig. 4B

FIG. 4A

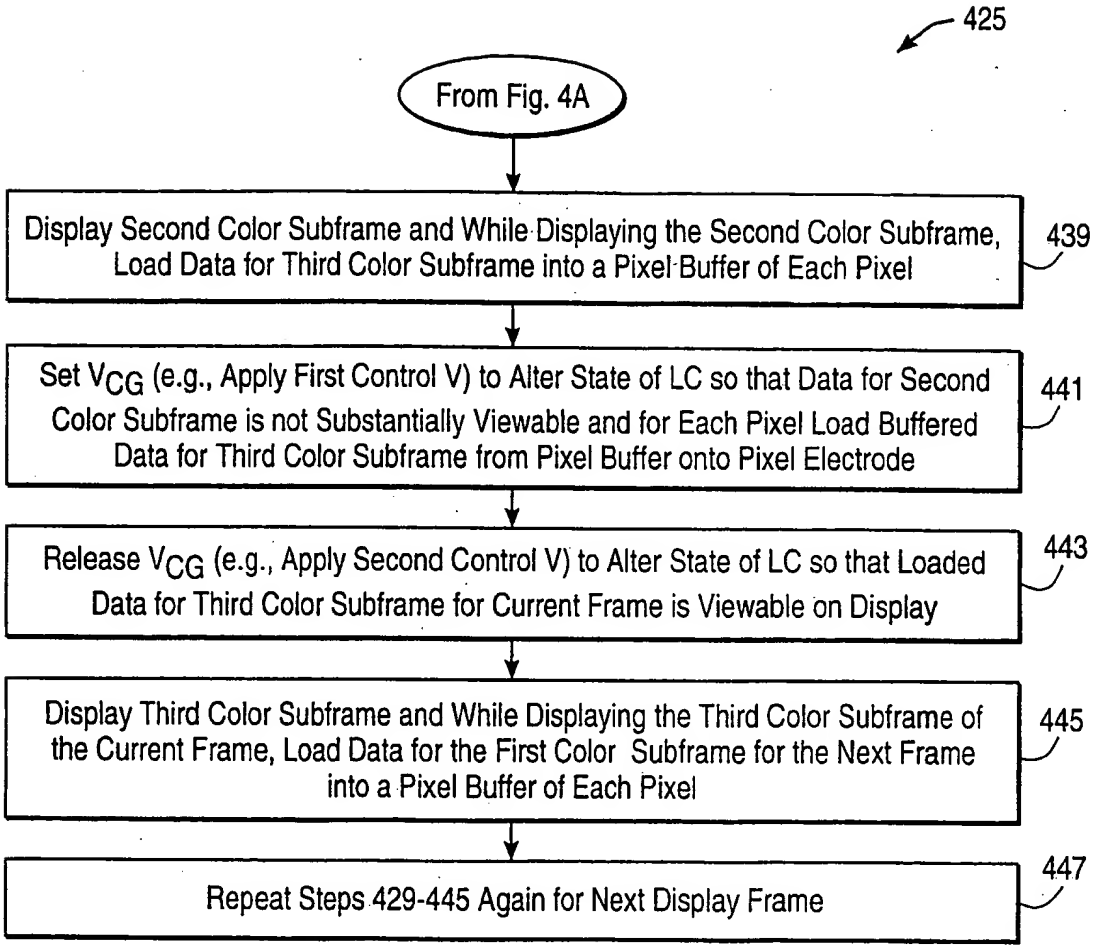

425
From Fig. 4A
Display Second Color Subframe and While Displaying the Second Color Subframe, Load Data for Third Color Subframe into a Pixel Buffer of Each Pixel
439
Set V_{CG} (e.g., Apply First Control V) to Alter State of LC so that Data for Second Color Subframe is not Substantially Viewable and for Each Pixel Load Buffered Data for Third Color Subframe from Pixel Buffer onto Pixel Electrode
441
Release V_{CG} (e.g., Apply Second Control V) to Alter State of LC so that Loaded Data for Third Color Subframe for Current Frame is Viewable on Display
443
Display Third Color Subframe and While Displaying the Third Color Subframe of the Current Frame, Load Data for the First Color Subframe for the Next Frame into a Pixel Buffer of Each Pixel
445
Repeat Steps 429-445 Again for Next Display Frame
447

FIG. 4B

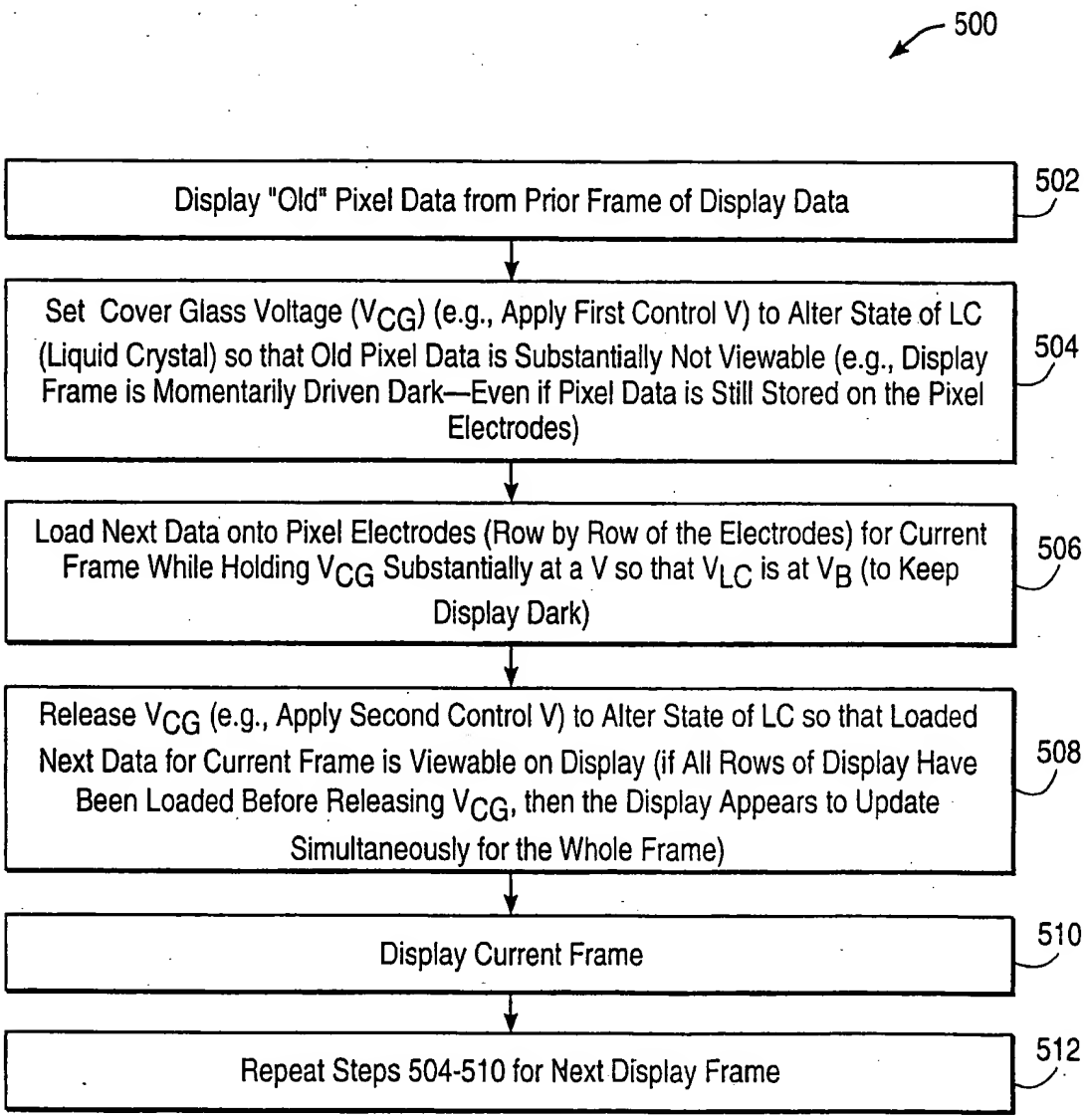

500
Display "Old" Pixel Data from Prior Frame of Display Data
502
Set Cover Glass Voltage (V_{CG}) (e.g., Apply First Control V) to Alter State of LC (Liquid Crystal) so that Old Pixel Data is Substantially Not Viewable (e.g., Display Frame is Momentarily Driven Dark—Even if Pixel Data is Still Stored on the Pixel Electrodes)
504
Load Next Data onto Pixel Electrodes (Row by Row of the Electrodes) for Current Frame While Holding V_{CG} Substantially at a V so that V_{LC} is at V_B (to Keep Display Dark)
506
Release V_{CG} (e.g., Apply Second Control V) to Alter State of LC so that Loaded Next Data for Current Frame is Viewable on Display (if All Rows of Display Have Been Loaded Before Releasing V_{CG}, then the Display Appears to Update Simultaneously for the Whole Frame)
508
Display Current Frame
510
Repeat Steps 504-510 for Next Display Frame
512

FIG. 5

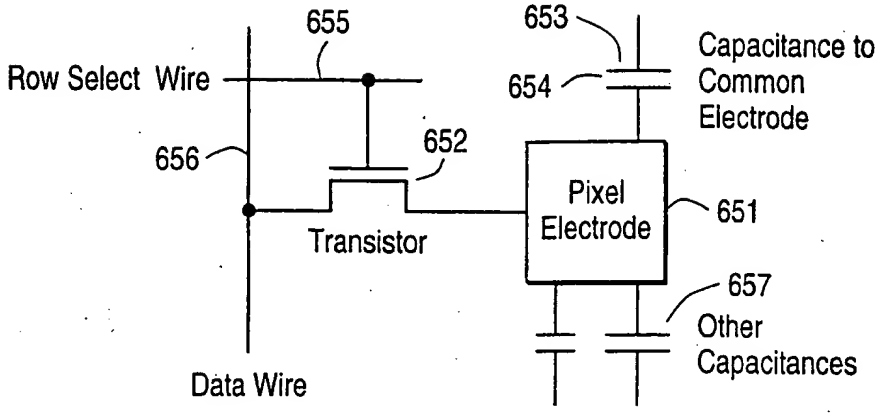


FIG. 6A

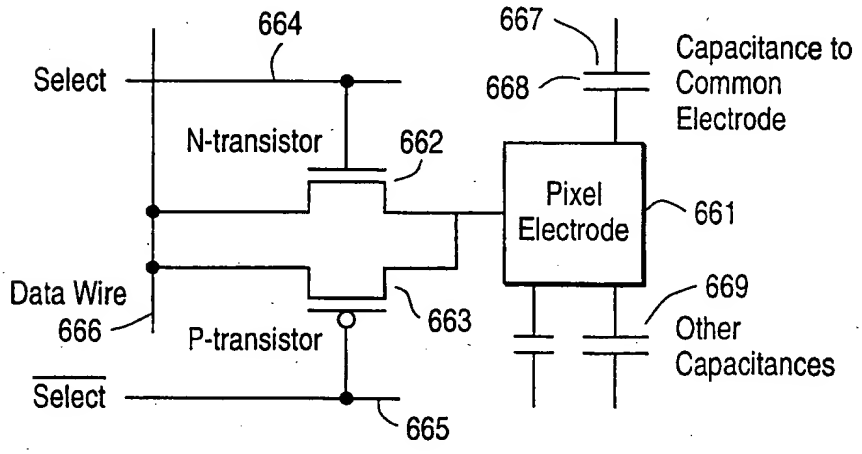


FIG. 6B

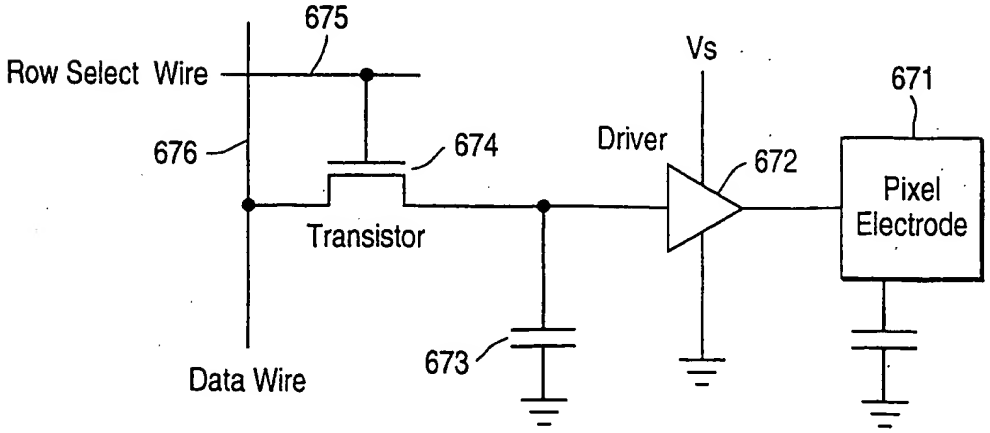


FIG. 6C

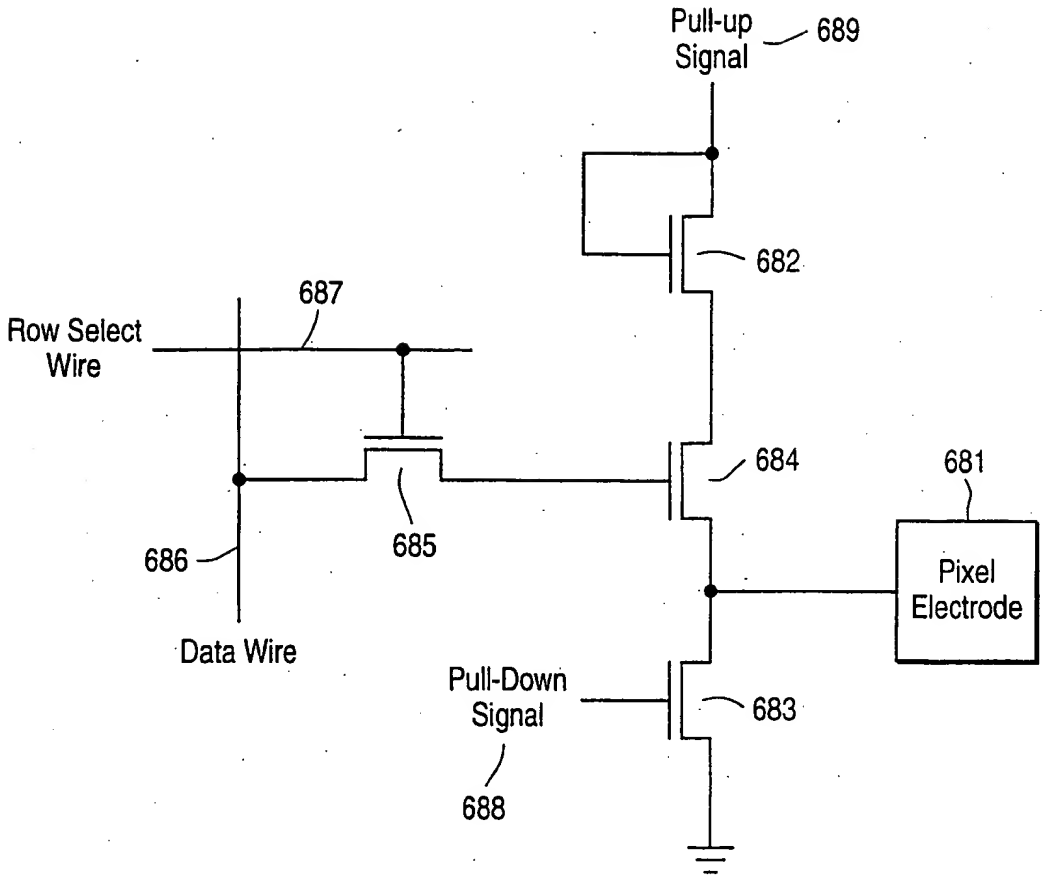

Pull-up
Signal
689
682
687
Row Select
Wire
684
681
685
686
Pixel
Electrode
Data Wire
Pull-Down
Signal
683
688

FIG. 6D

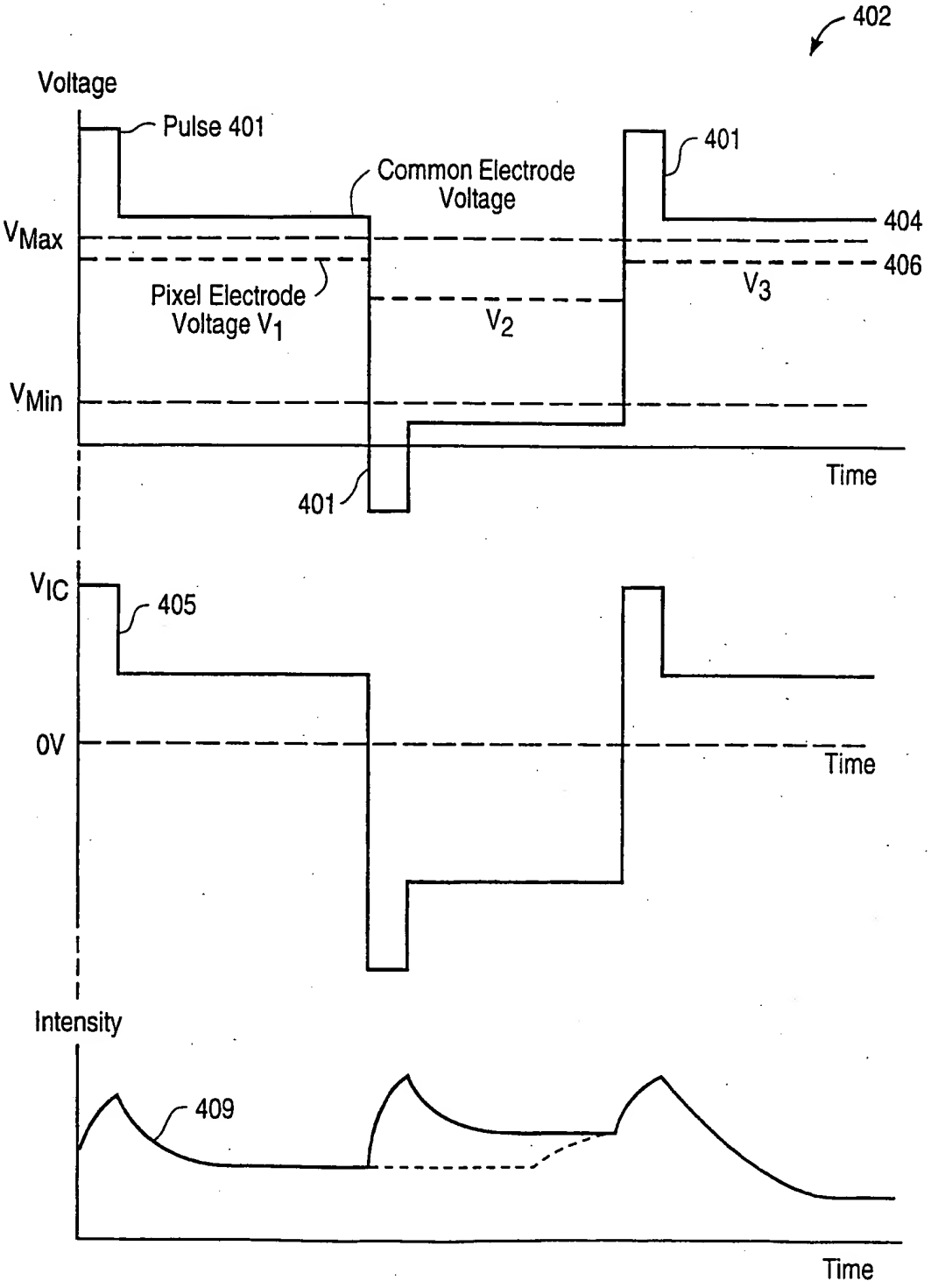

402
Voltage
Pulse 401
401
Common Electrode Voltage
404
406
V_{Max}
Pixel Electrode Voltage V_1
V_2
V_3
V_{Min}
401
Time
V_{IC}
405
0V
Time
Intensity
409
Time

FIG. 7A

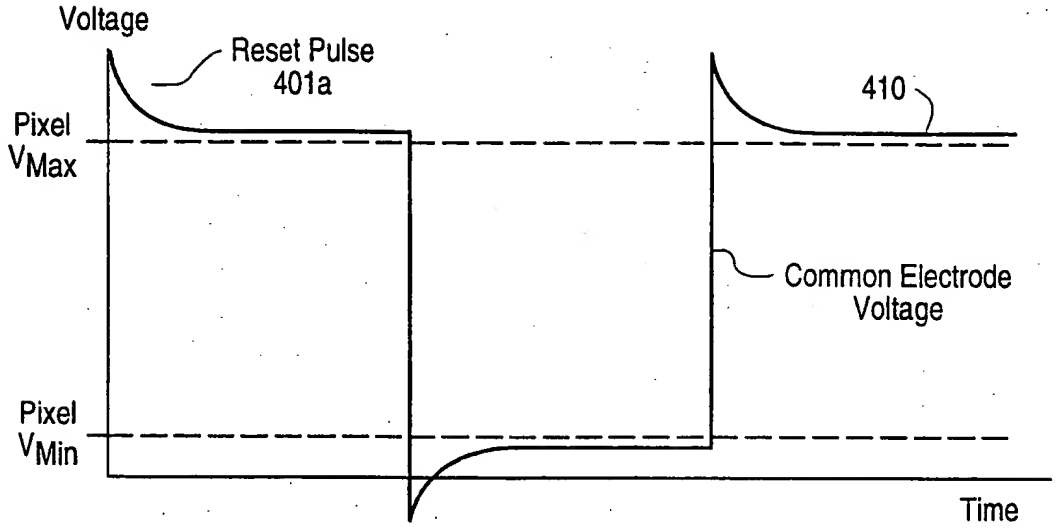

Voltage
Reset Pulse
401a
410
Pixel
V_{Max}
Common Electrode
Voltage
Pixel
V_{Min}
Time

FIG. 7B

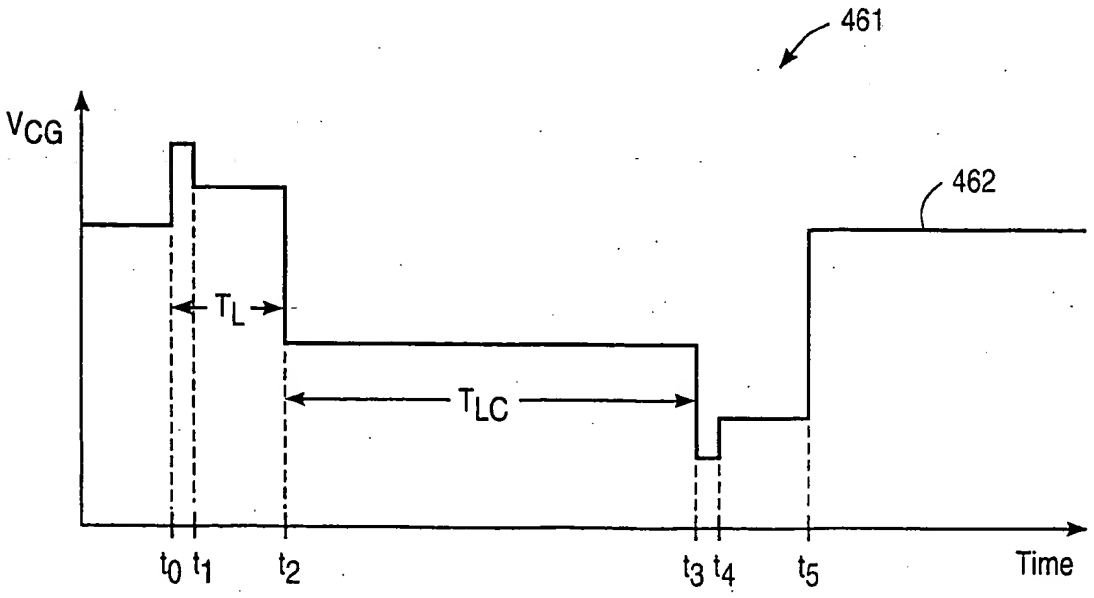

461
V_{CG}
462
T_L
T_{LC}
t_0 t_1 t_2 t_3 t_4 t_5
Time

FIG. 7C

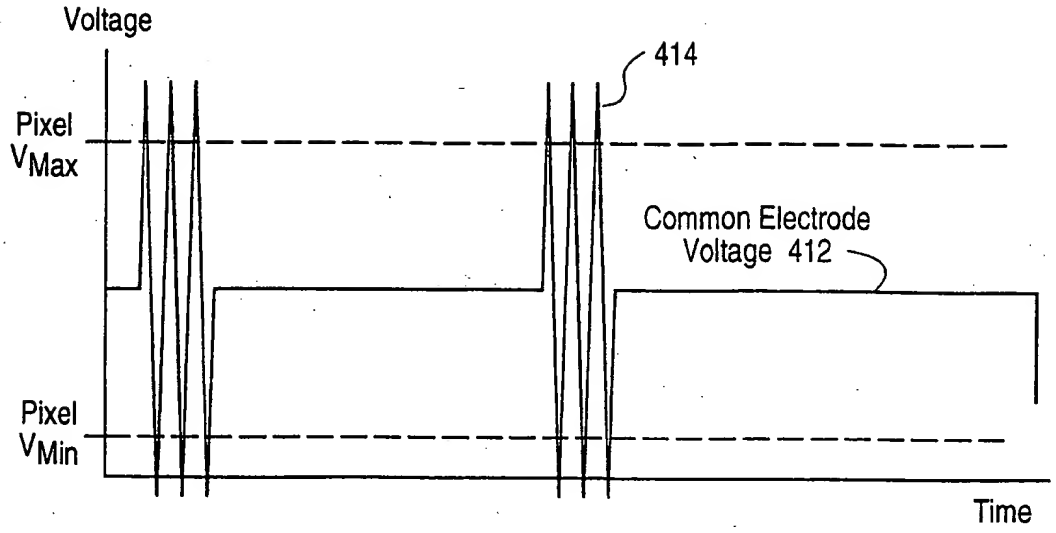

Voltage
414
Pixel
V_{Max}
Common Electrode
Voltage 412
Pixel
V_{Min}
Time

FIG. 8A

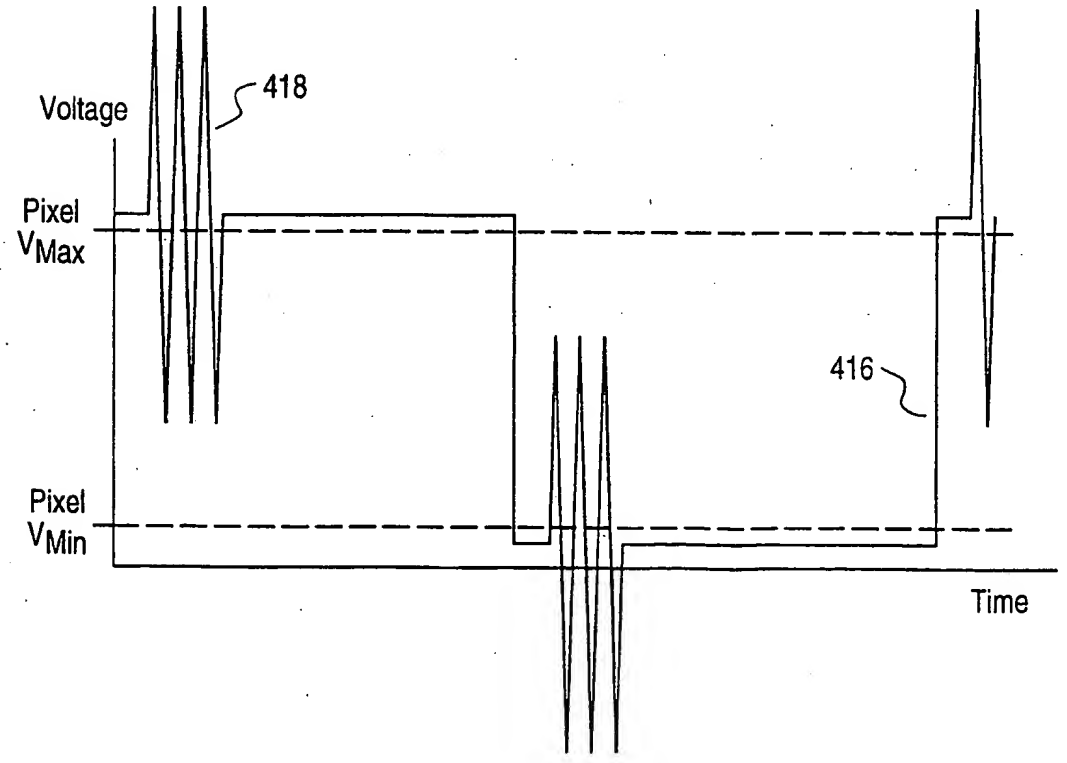

Voltage
418
Pixel
V_{Max}
416
Pixel
V_{Min}
Time

FIG. 8B

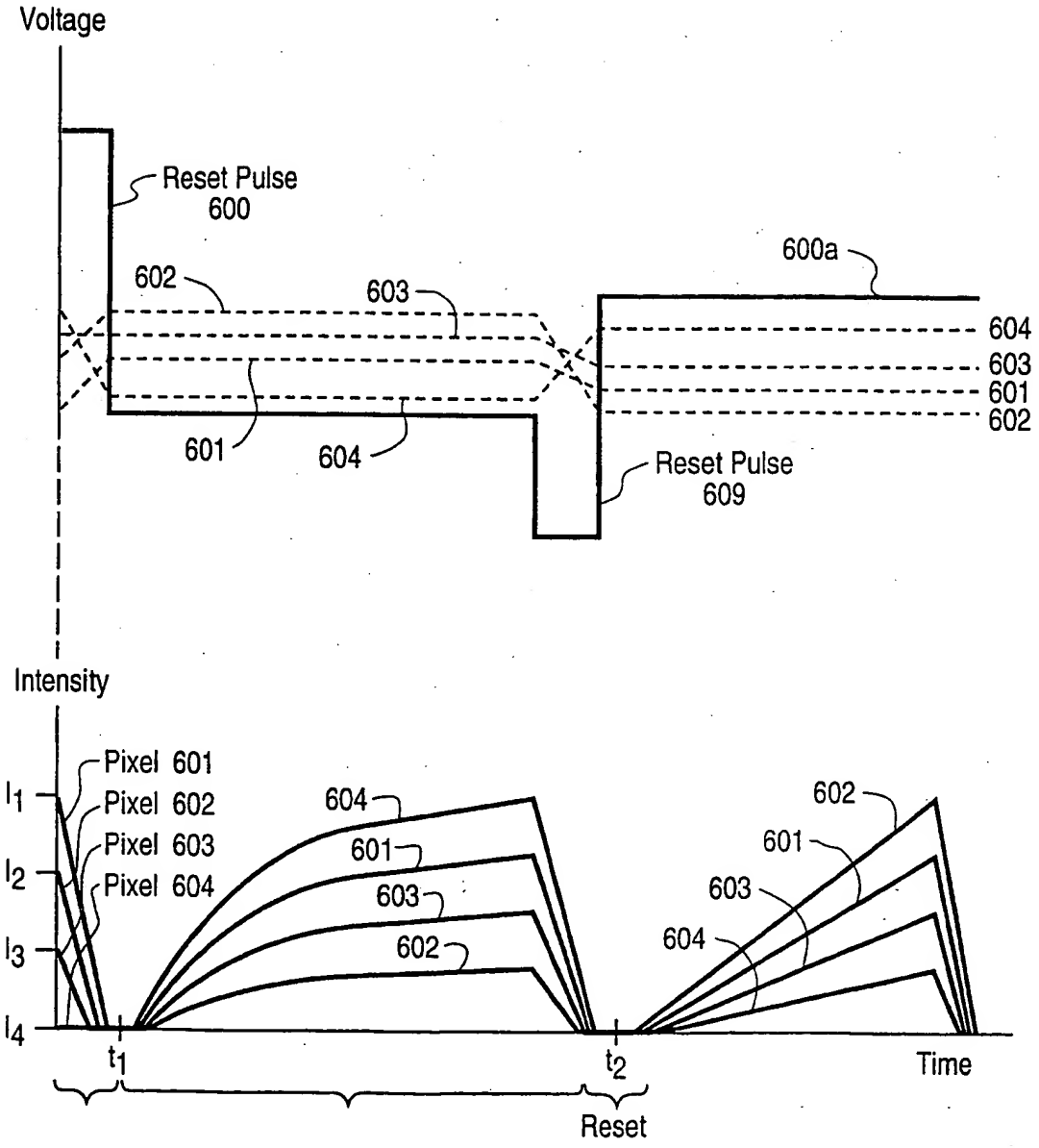

Voltage
Reset Pulse
600
602
603
600a
604
603
601
602
601
604
Reset Pulse
609
Intensity
Pixel 601
Pixel 602
Pixel 603
Pixel 604
I1
I2
I3
I4
604
601
603
602
602
601
603
604
t1
t2
Time
Reset

FIG. 9A

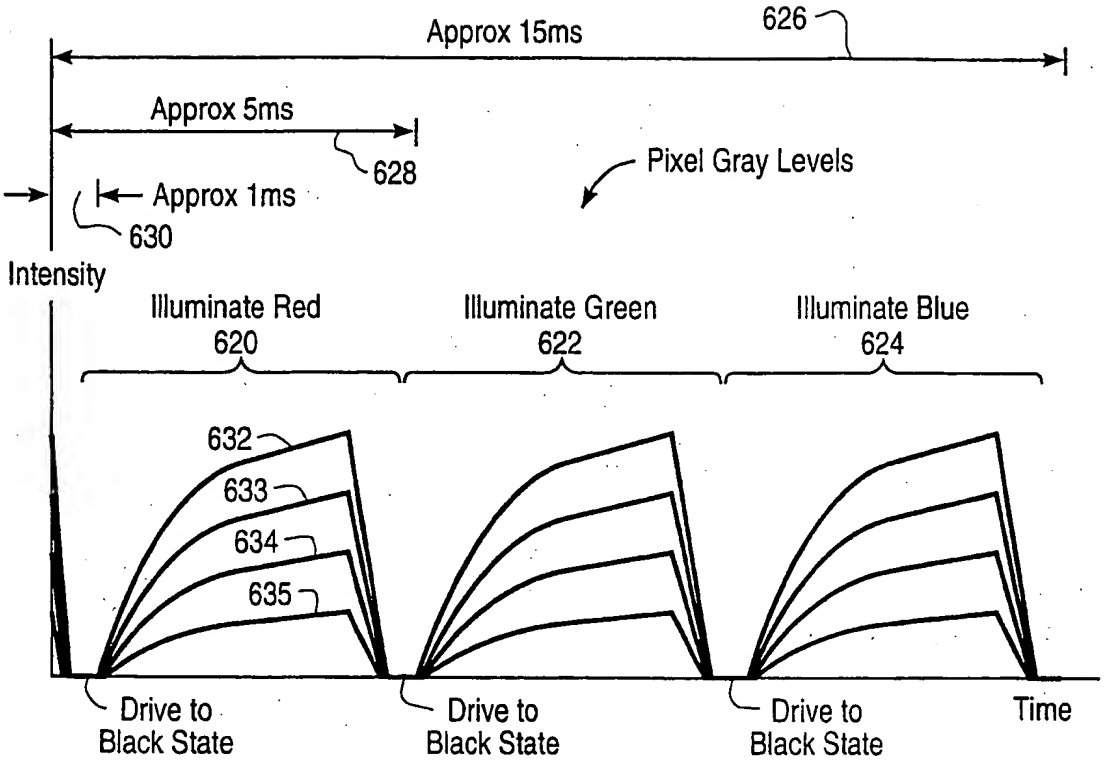

Approx 15ms
626
Approx 5ms
628
Pixel Gray Levels
Approx 1ms
630
Intensity
Illuminate Red
620
Illuminate Green
622
Illuminate Blue
624
632
633
634
635
Drive to Black State
Drive to Black State
Drive to Black State
Time

FIG. 9B

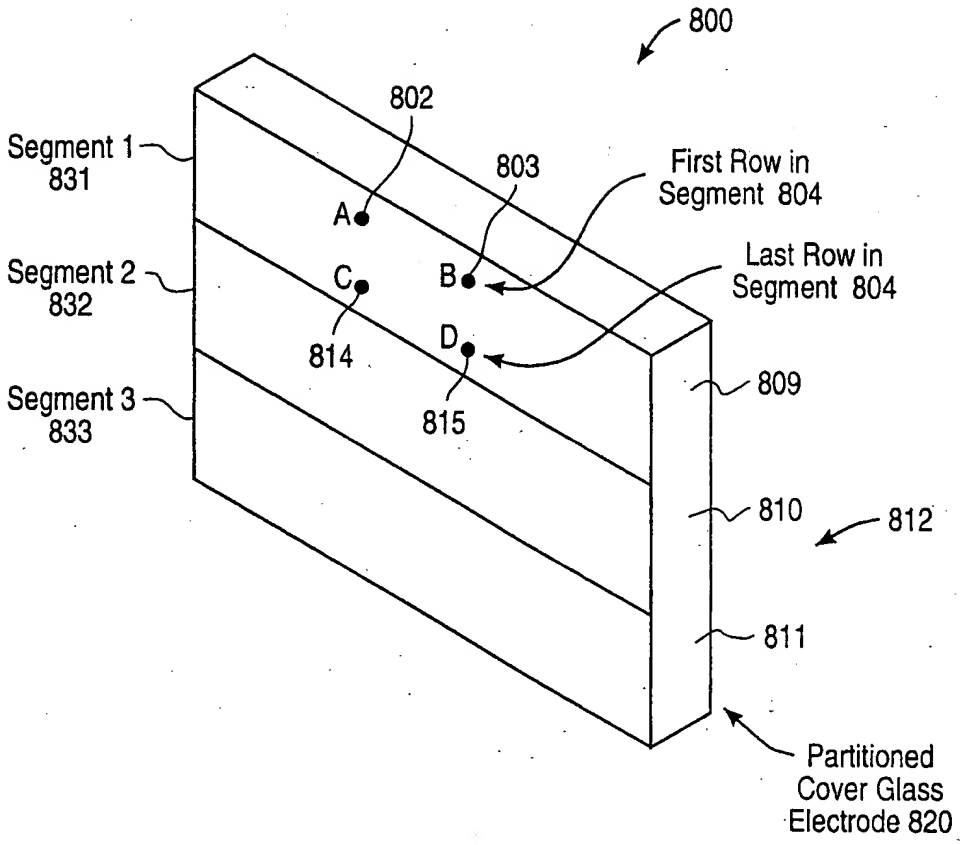

800
802
803
First Row in
Segment 804
Last Row in
Segment 804
Segment 1
831
Segment 2
832
Segment 3
833
A
B
C
D
814
815
809
810
812
811
Partitioned
Cover Glass
Electrode 820

FIG. 10A

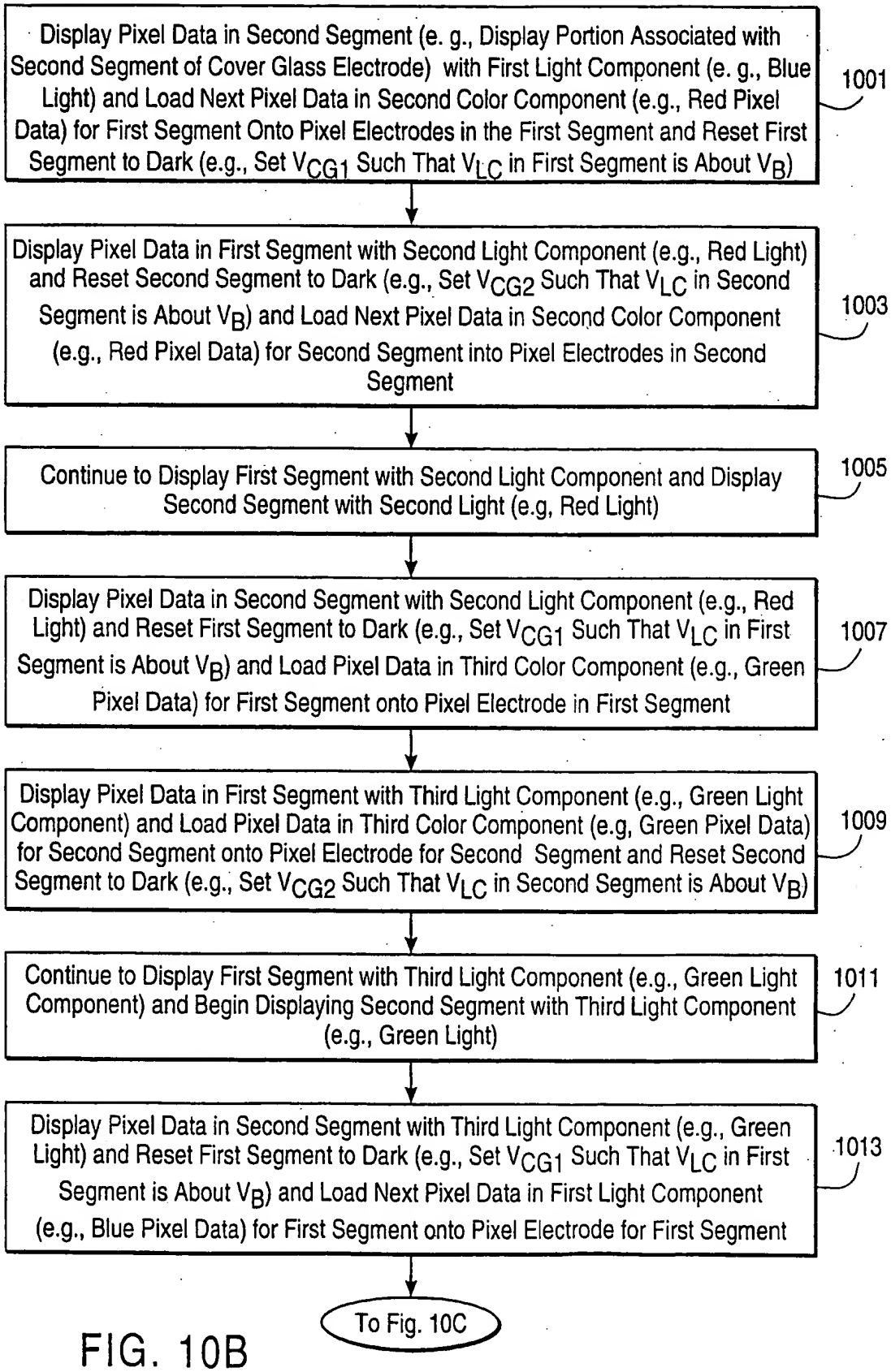

Display Pixel Data in Second Segment (e. g., Display Portion Associated with Second Segment of Cover Glass Electrode) with First Light Component (e. g., Blue Light) and Load Next Pixel Data in Second Color Component (e.g., Red Pixel Data) for First Segment Onto Pixel Electrodes in the First Segment and Reset First Segment to Dark (e.g., Set V_{CG1} Such That V_{LC} in First Segment is About V_B)
1001
Display Pixel Data in First Segment with Second Light Component (e.g., Red Light) and Reset Second Segment to Dark (e.g., Set V_{CG2} Such That V_{LC} in Second Segment is About V_B) and Load Next Pixel Data in Second Color Component (e.g., Red Pixel Data) for Second Segment into Pixel Electrodes in Second Segment
1003
Continue to Display First Segment with Second Light Component and Display Second Segment with Second Light (e.g, Red Light)
1005
Display Pixel Data in Second Segment with Second Light Component (e.g., Red Light) and Reset First Segment to Dark (e.g., Set V_{CG1} Such That V_{LC} in First Segment is About V_B) and Load Pixel Data in Third Color Component (e.g., Green Pixel Data) for First Segment onto Pixel Electrode in First Segment
1007
Display Pixel Data in First Segment with Third Light Component (e.g., Green Light Component) and Load Pixel Data in Third Color Component (e.g, Green Pixel Data) for Second Segment onto Pixel Electrode for Second Segment and Reset Second Segment to Dark (e.g., Set V_{CG2} Such That V_{LC} in Second Segment is About V_B)
1009
Continue to Display First Segment with Third Light Component (e.g., Green Light Component) and Begin Displaying Second Segment with Third Light Component (e.g., Green Light)
1011
Display Pixel Data in Second Segment with Third Light Component (e.g., Green Light) and Reset First Segment to Dark (e.g., Set V_{CG1} Such That V_{LC} in First Segment is About V_B) and Load Next Pixel Data in First Light Component (e.g., Blue Pixel Data) for First Segment onto Pixel Electrode for First Segment
1013
To Fig. 10C

FIG. 10B

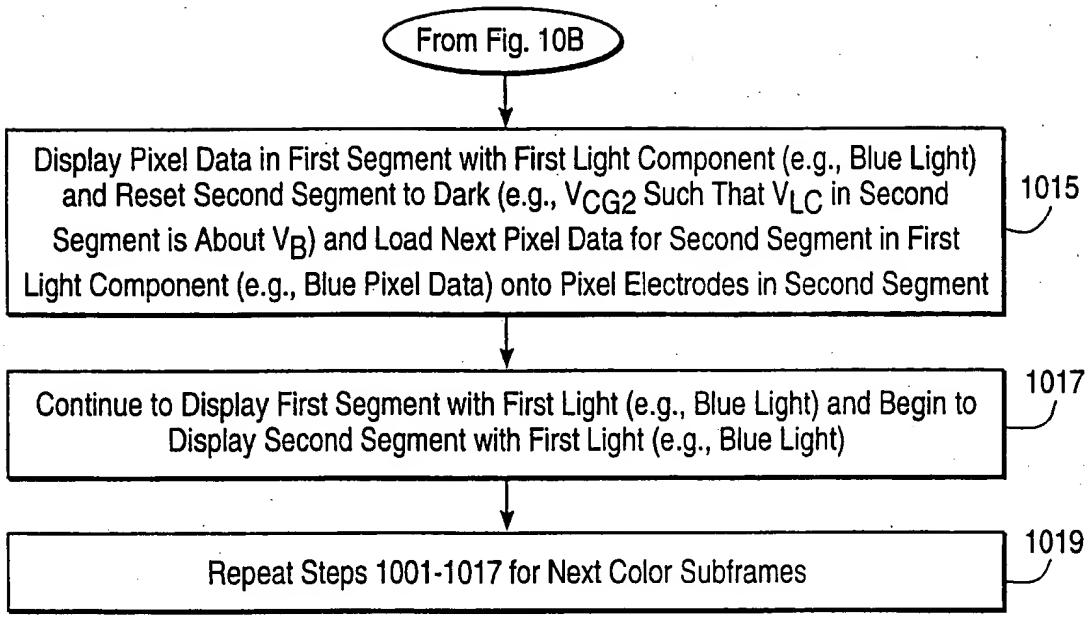

From Fig. 10B
Display Pixel Data in First Segment with First Light Component (e.g., Blue Light) and Reset Second Segment to Dark (e.g., V_{CG2} Such That V_{LC} in Second Segment is About V_B) and Load Next Pixel Data for Second Segment in First Light Component (e.g., Blue Pixel Data) onto Pixel Electrodes in Second Segment
1015
Continue to Display First Segment with First Light (e.g., Blue Light) and Begin to Display Second Segment with First Light (e.g., Blue Light)
1017
Repeat Steps 1001-1017 for Next Color Subframes
1019

FIG. 10C

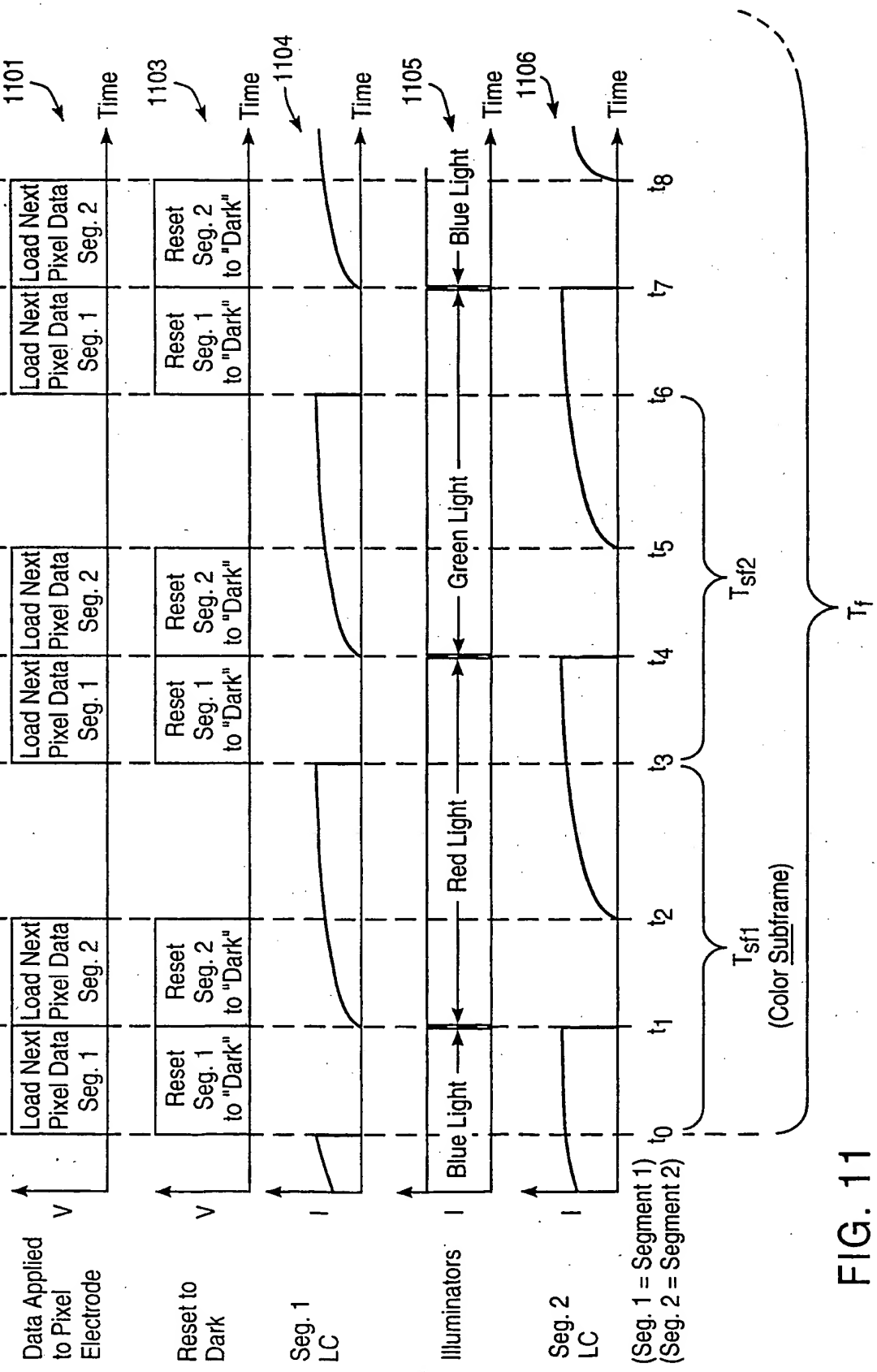

Data Applied to Pixel Electrode
Reset to Dark
Seg. 1 LC
Illuminators
Seg. 2 LC
(Seg. 1 = Segment 1)
(Seg. 2 = Segment 2)
V
I
Time
1101
1103
1104
1105
1106
Load Next Pixel Data Seg. 1
Load Next Pixel Data Seg. 2
Reset Seg. 1 to "Dark"
Reset Seg. 2 to "Dark"
Blue Light
Red Light
Green Light
t_0
t_1
t_2
t_3
t_4
t_5
t_6
t_7
t_8
T_{sf1}
(Color Subframe)
T_{sf2}
T_f

FIG. 11

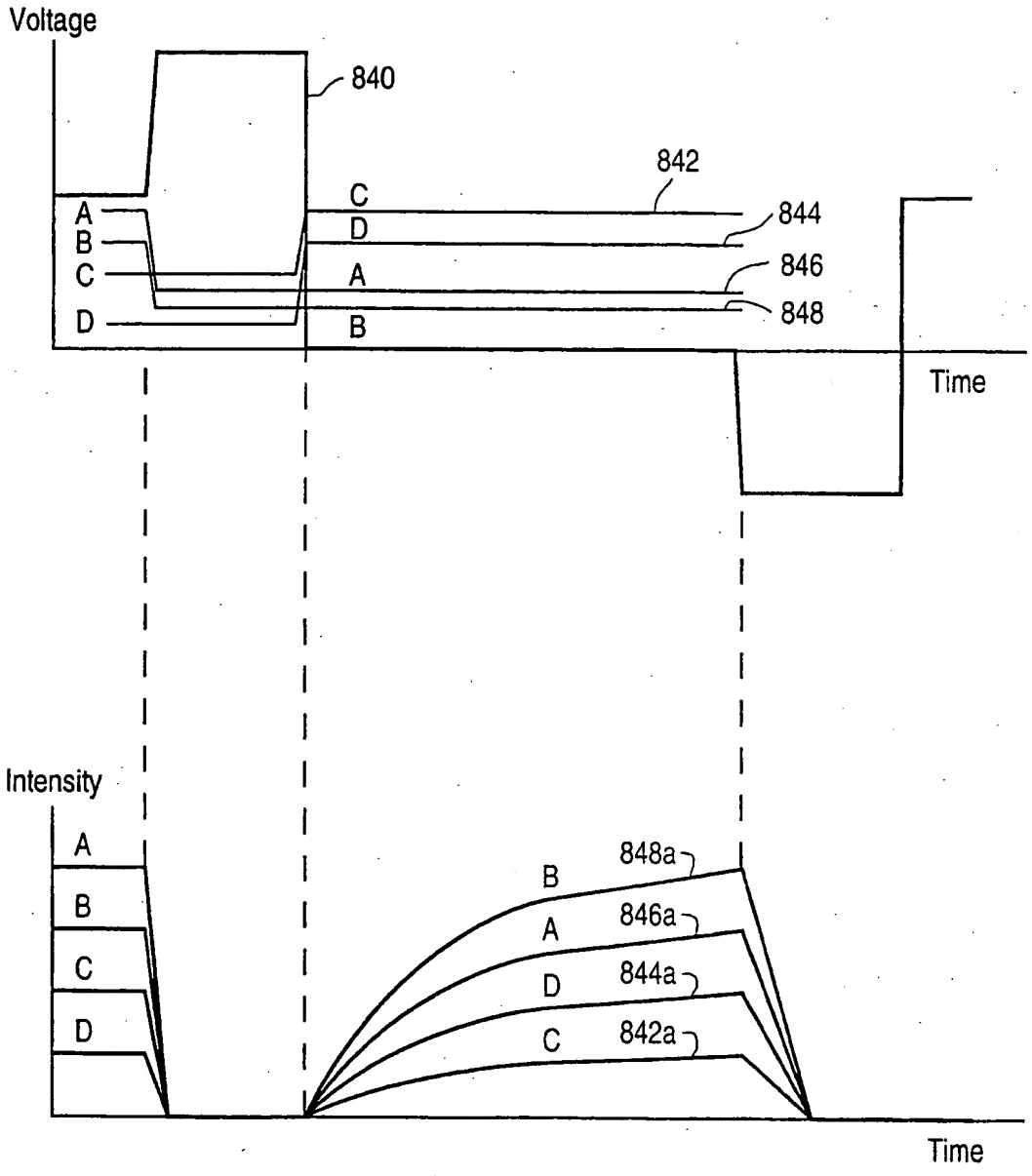

Voltage
840
842
A
B
C
D
C
D
A
B
844
846
848
Time
Intensity
A
B
C
D
B
A
D
C
848a
846a
844a
842a
Time

FIG. 12

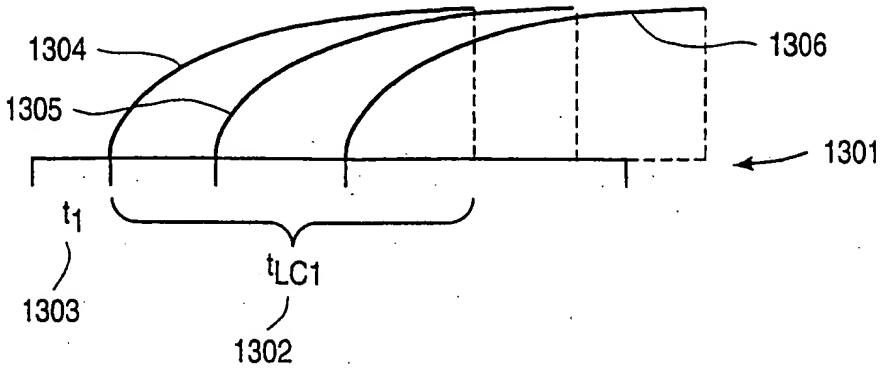


FIG. 13A

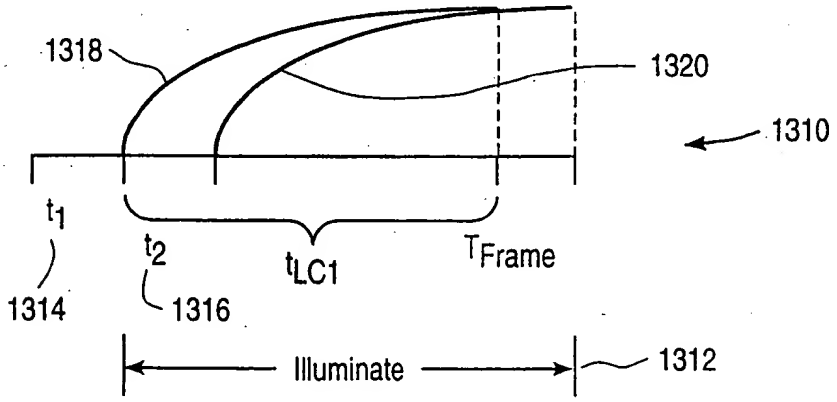


FIG. 13B

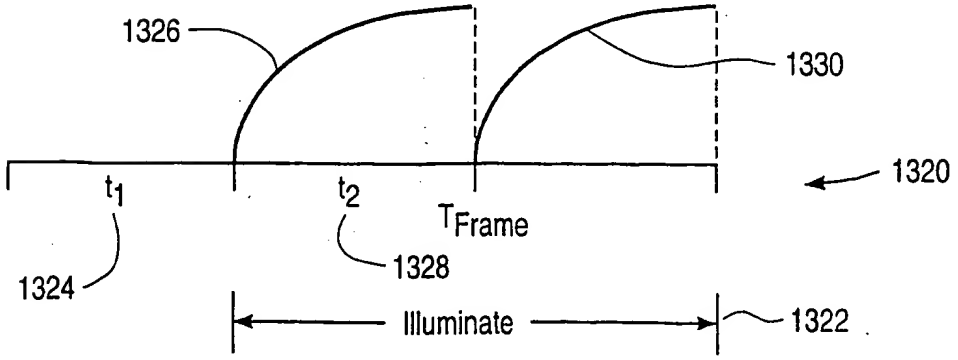


FIG. 13C

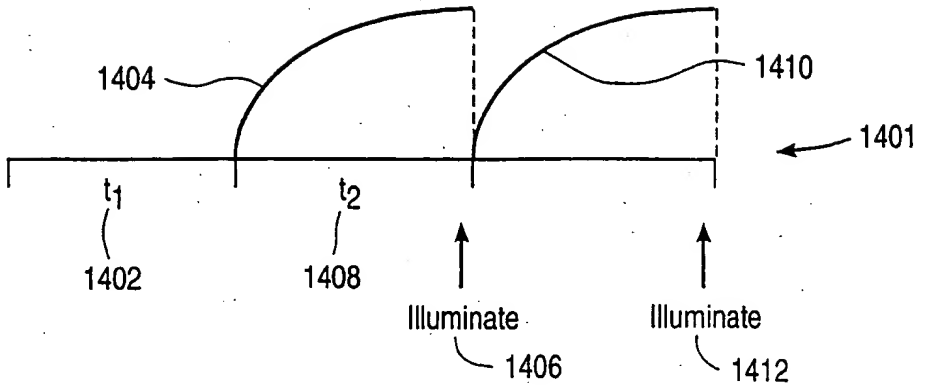


FIG. 14

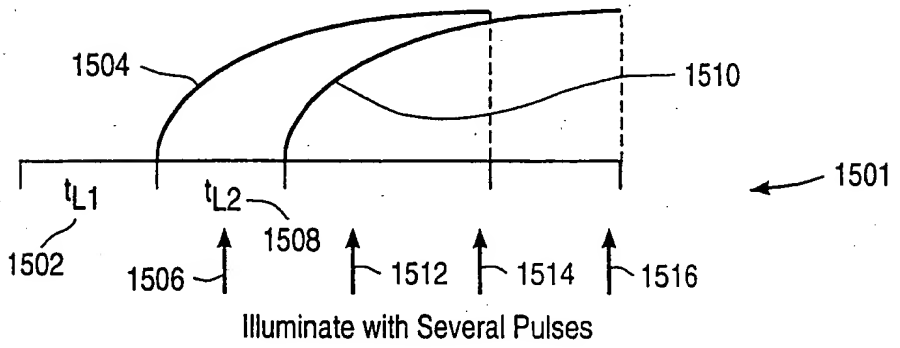


FIG. 15

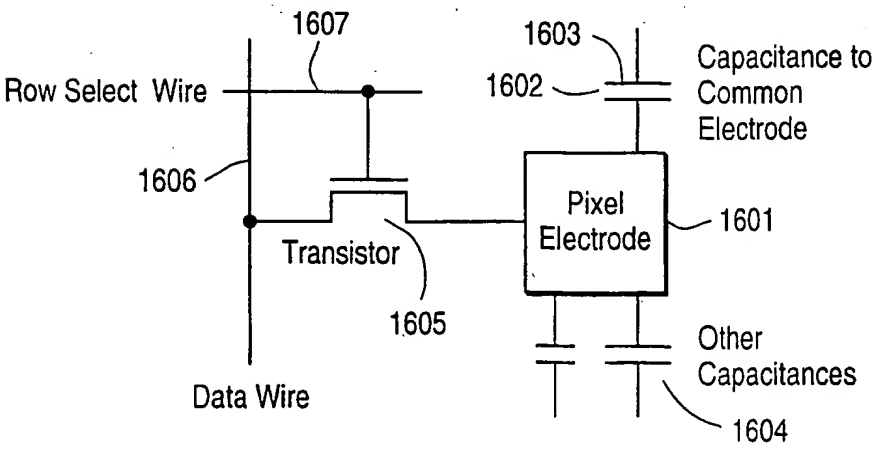


FIG. 16A

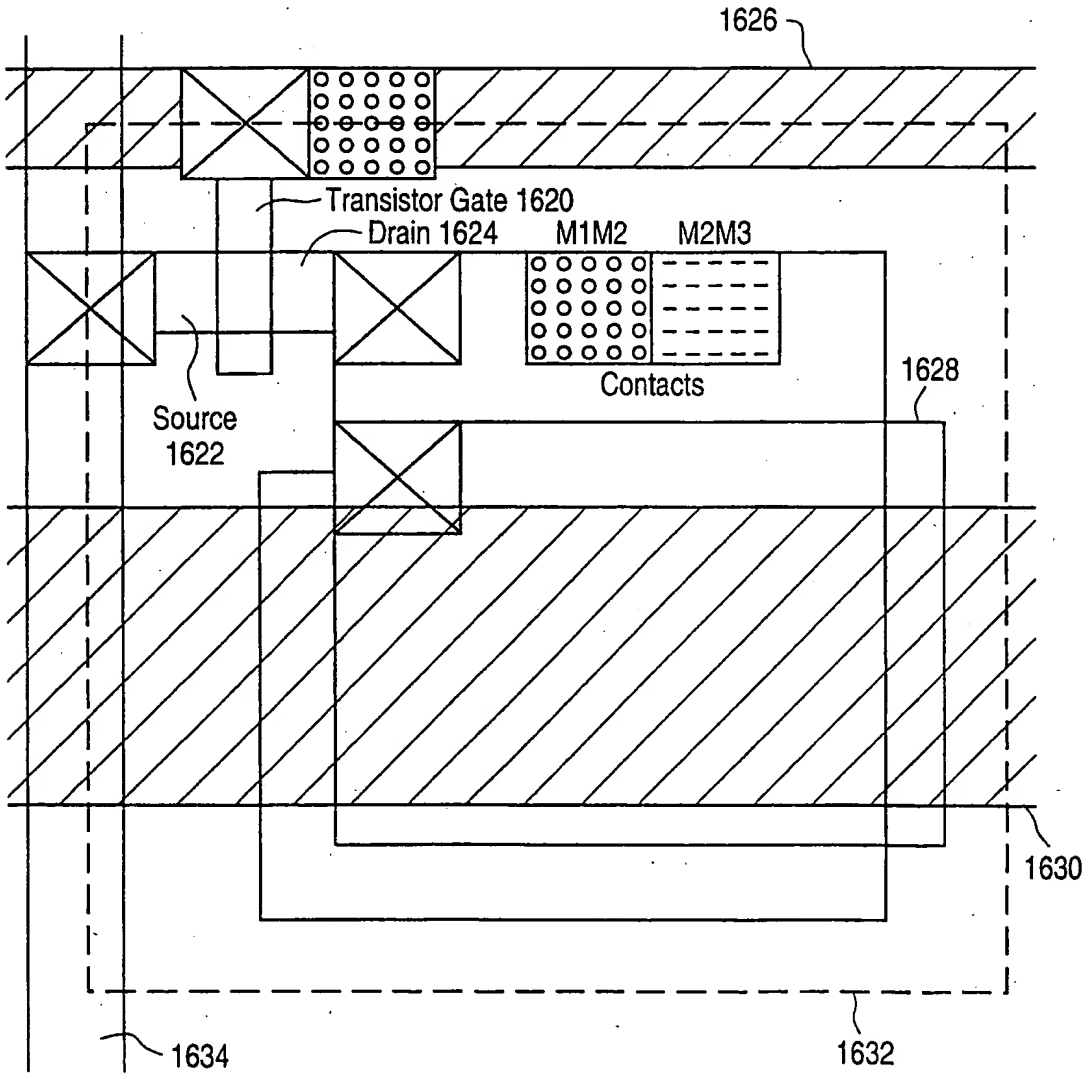

1626
Transistor Gate 1620
Drain 1624
M1M2
M2M3
Contacts
1628
Source
1622
1630
1634
1632

FIG. 16B

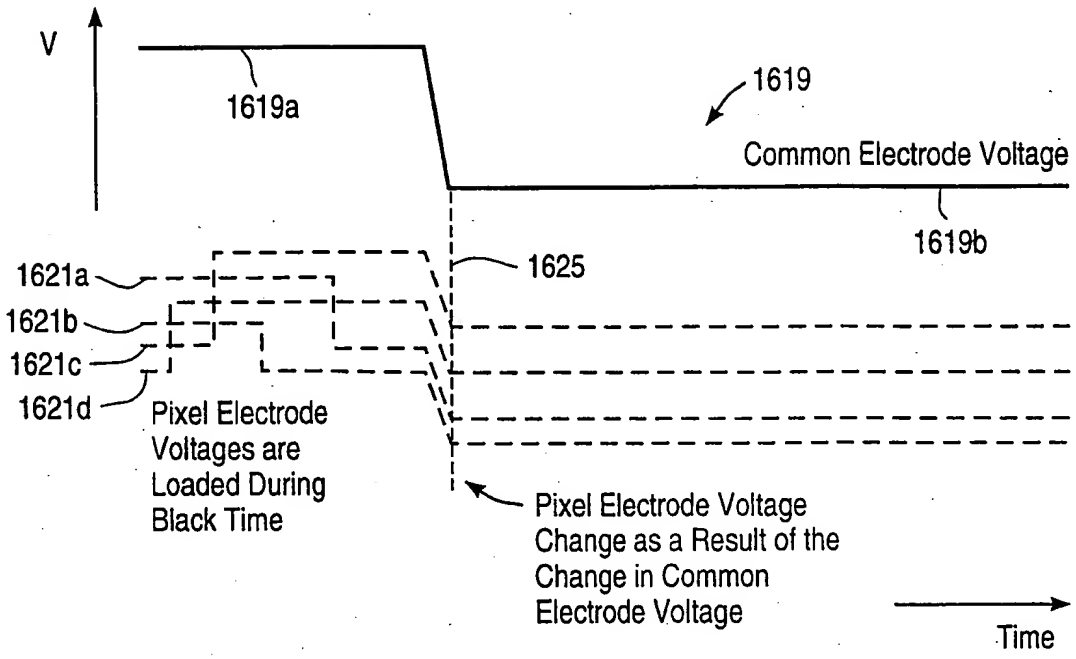


FIG. 16C

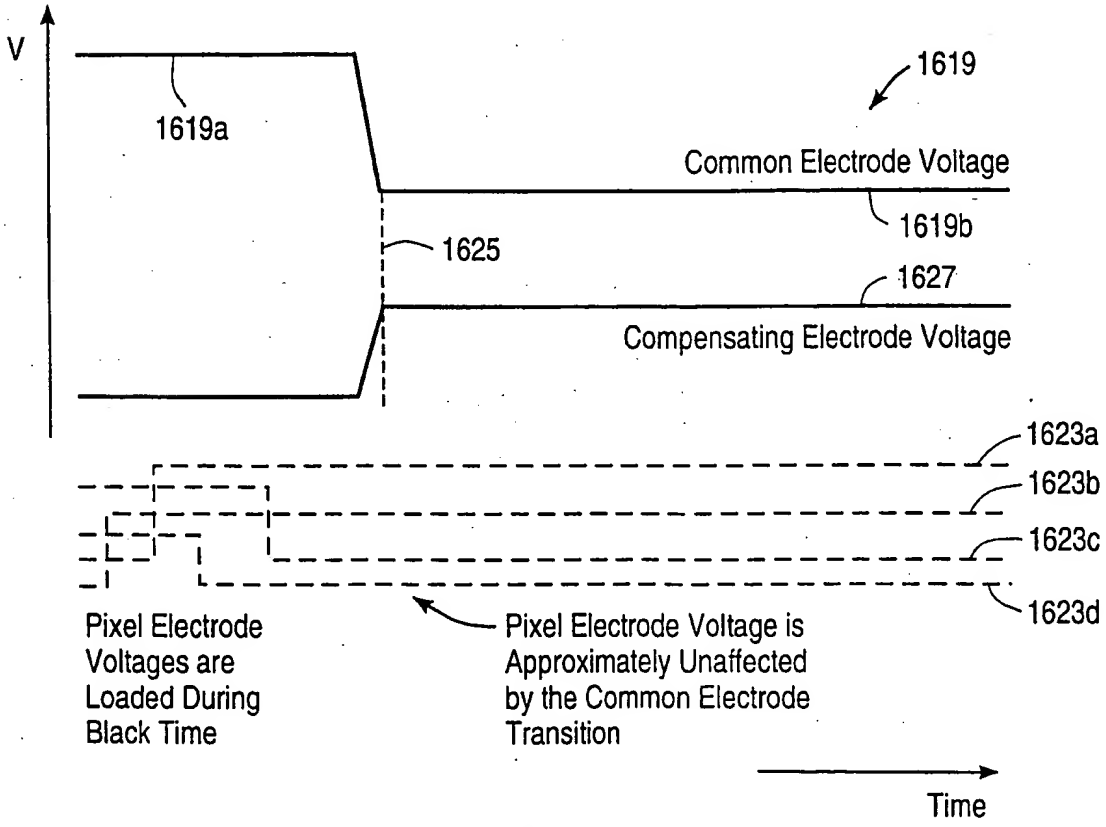


FIG. 16D

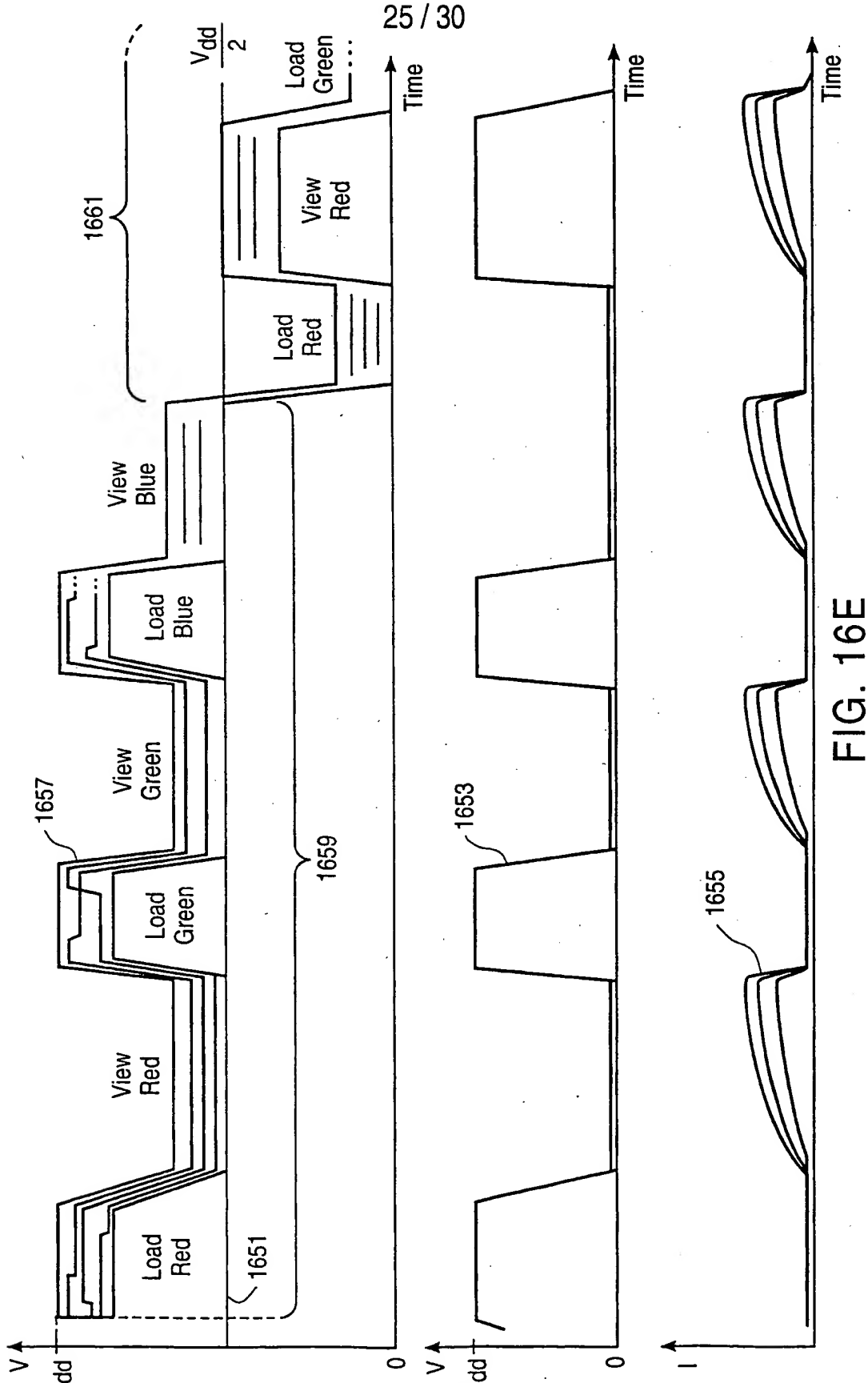

V
V_{dd}
0
Time
1651
1653
1655
1657
1659
1661
Load Red
View Red
Load Green
View Green
Load Blue
View Blue
$\frac{V_{dd}}{2}$
I

FIG. 16E

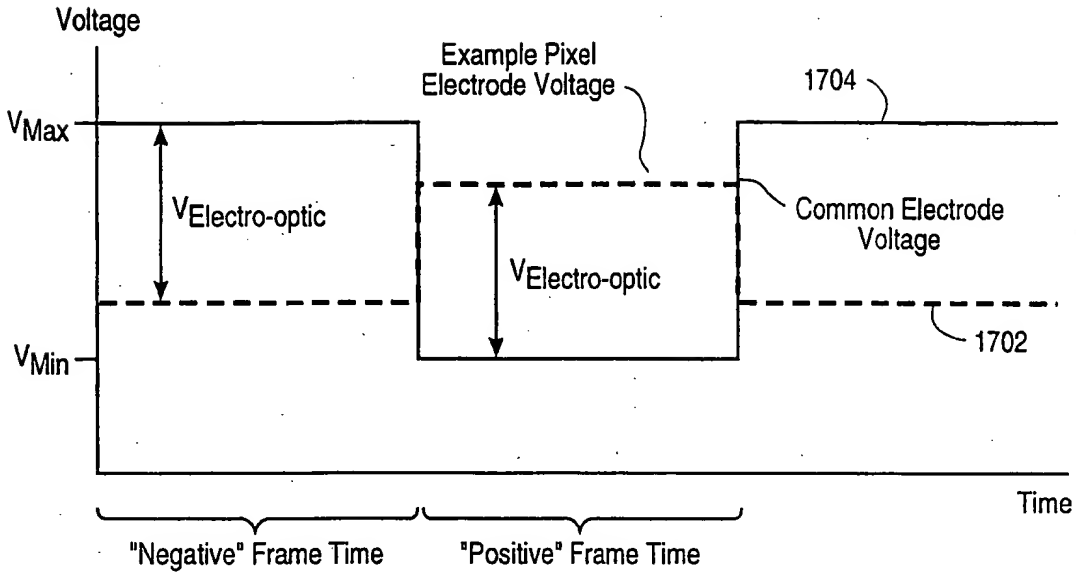

Voltage
Example Pixel
Electrode Voltage
1704
V_{Max}
$V_{Electro\text{-}optic}$
$V_{Electro\text{-}optic}$
Common Electrode
Voltage
1702
V_{Min}
Time
"Negative" Frame Time
"Positive" Frame Time

FIG. 17

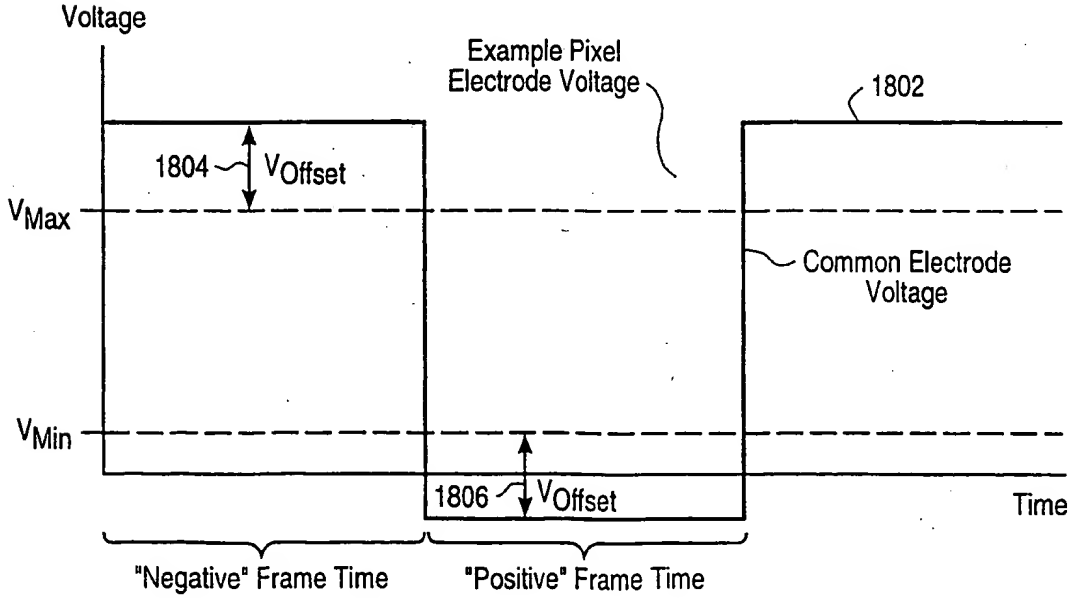

Voltage
Example Pixel
Electrode Voltage
1802
1804
V_{Offset}
V_{Max}
Common Electrode
Voltage
V_{Min}
1806
V_{Offset}
Time
"Negative" Frame Time
"Positive" Frame Time

FIG. 18

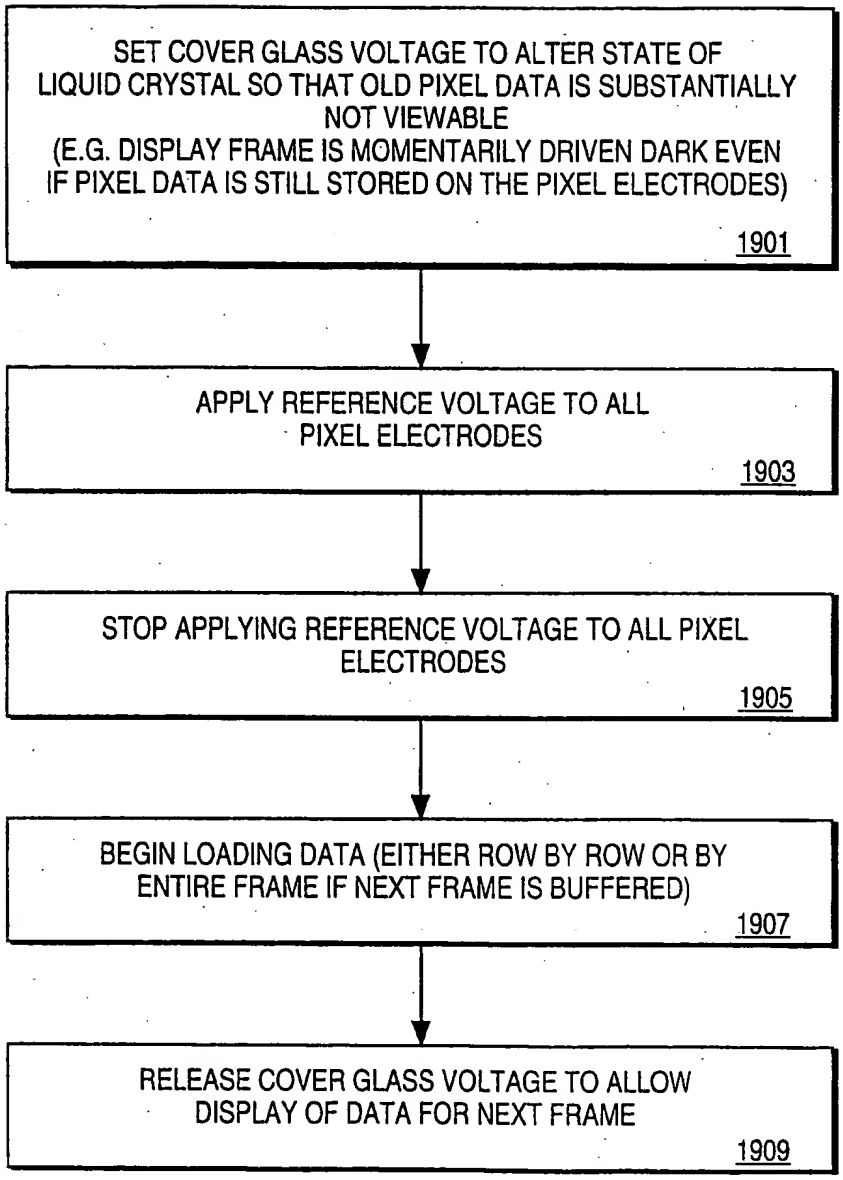

SET COVER GLASS VOLTAGE TO ALTER STATE OF LIQUID CRYSTAL SO THAT OLD PIXEL DATA IS SUBSTANTIALLY NOT VIEWABLE (E.G. DISPLAY FRAME IS MOMENTARILY DRIVEN DARK EVEN IF PIXEL DATA IS STILL STORED ON THE PIXEL ELECTRODES)
1901
APPLY REFERENCE VOLTAGE TO ALL PIXEL ELECTRODES
1903
STOP APPLYING REFERENCE VOLTAGE TO ALL PIXEL ELECTRODES
1905
BEGIN LOADING DATA (EITHER ROW BY ROW OR BY ENTIRE FRAME IF NEXT FRAME IS BUFFERED)
1907
RELEASE COVER GLASS VOLTAGE TO ALLOW DISPLAY OF DATA FOR NEXT FRAME
1909

FIG. 19

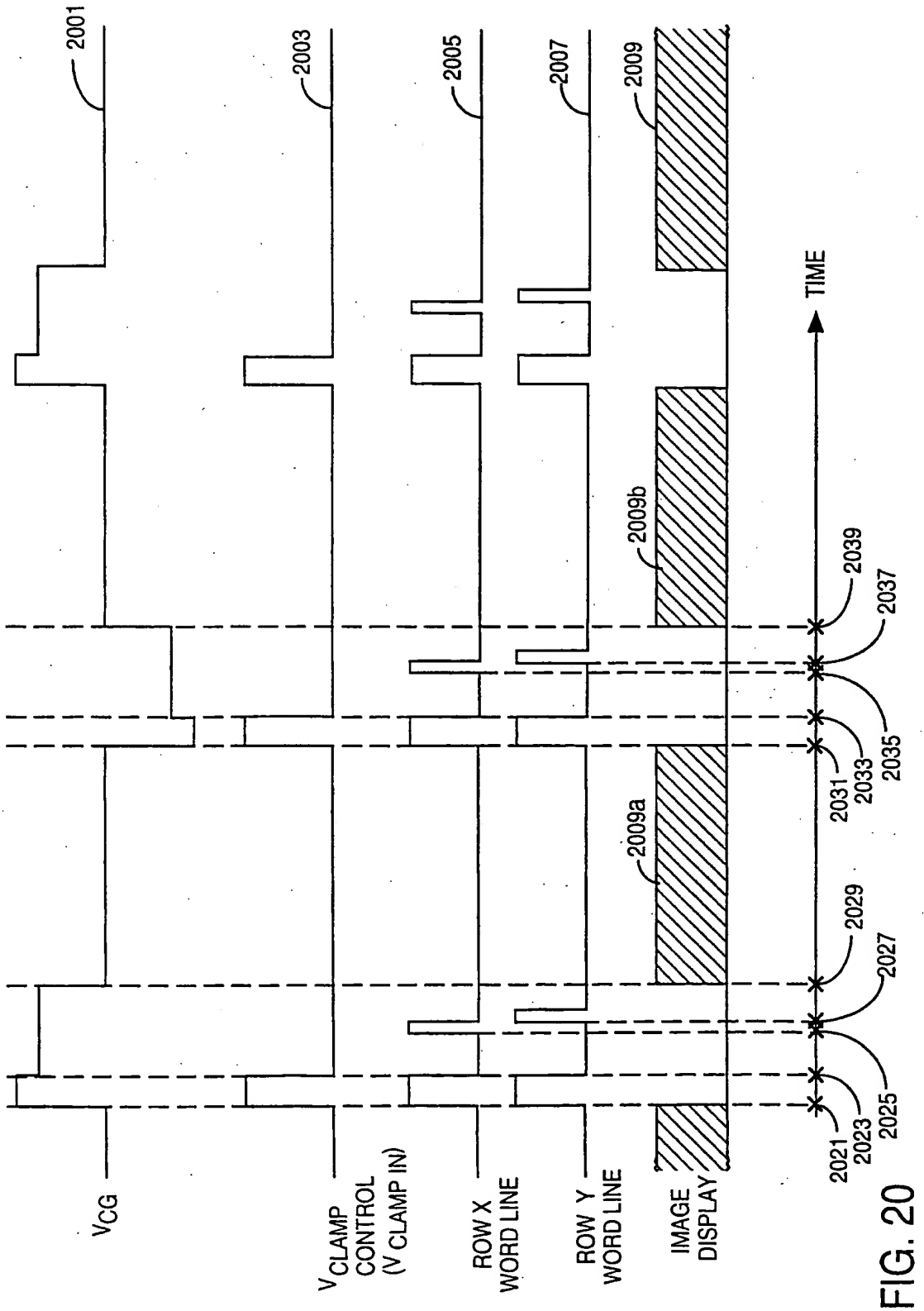

2001
2003
2005
2007
2009
2009b
2009a
TIME
2039
2037
2035
2033
2031
2029
2027
2025
2023
2021
V_{CG}
V_{CLAMP} CONTROL ($V_{CLAMP\ IN}$)
ROW X WORD LINE
ROW Y WORD LINE
IMAGE DISPLAY

FIG. 20

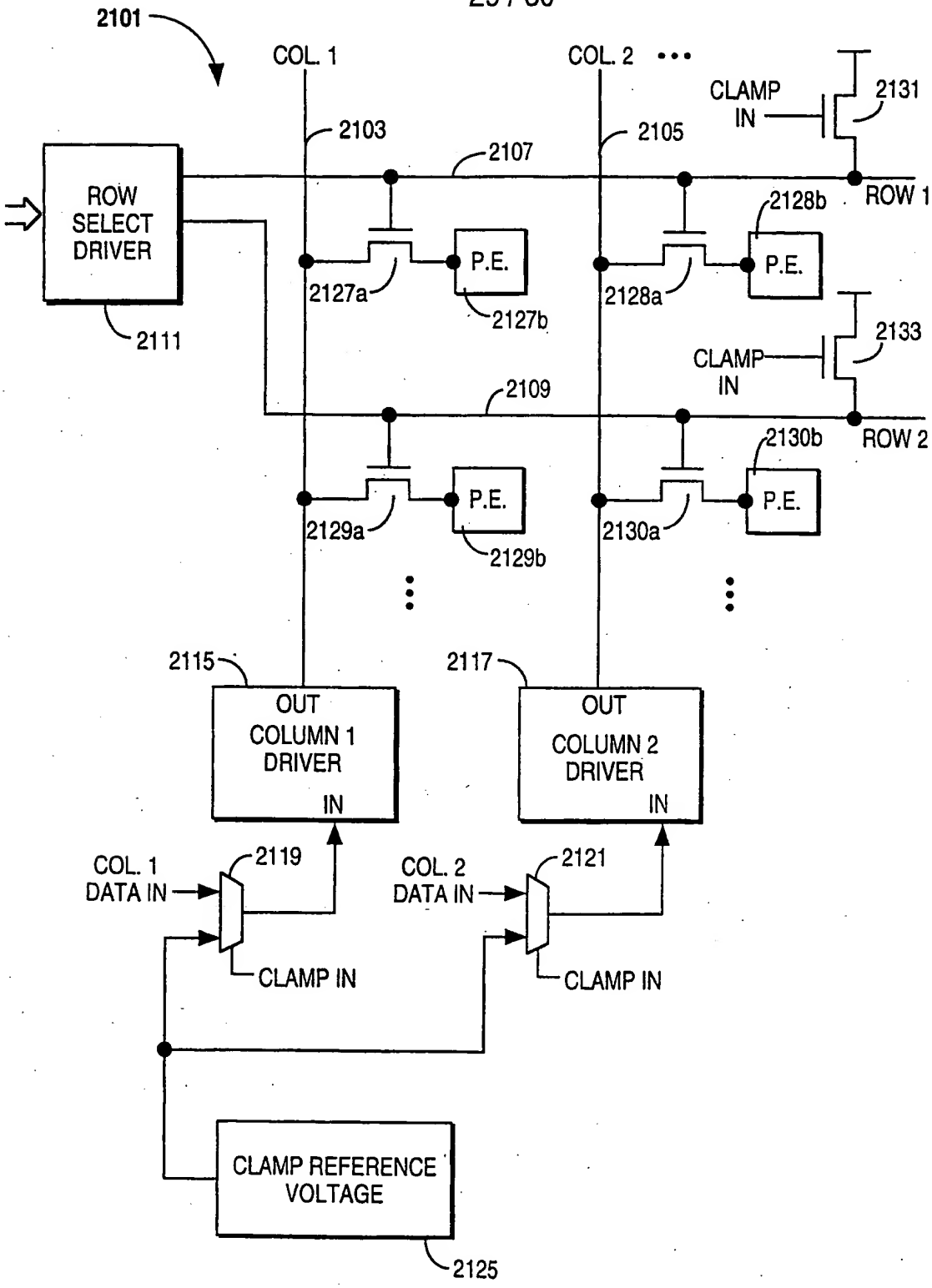

2101
COL. 1
COL. 2
CLAMP IN
2131
2103
2105
2107
ROW SELECT DRIVER
ROW 1
2128b
P.E.
2127a
2127b
2128a
2111
2133
CLAMP IN
2109
ROW 2
2130b
2129a
2129b
2130a
2115
2117
OUT COLUMN 1 DRIVER IN
OUT COLUMN 2 DRIVER IN
COL. 1 DATA IN
2119
COL. 2 DATA IN
2121
CLAMP IN
CLAMP REFERENCE VOLTAGE
2125

FIG. 21

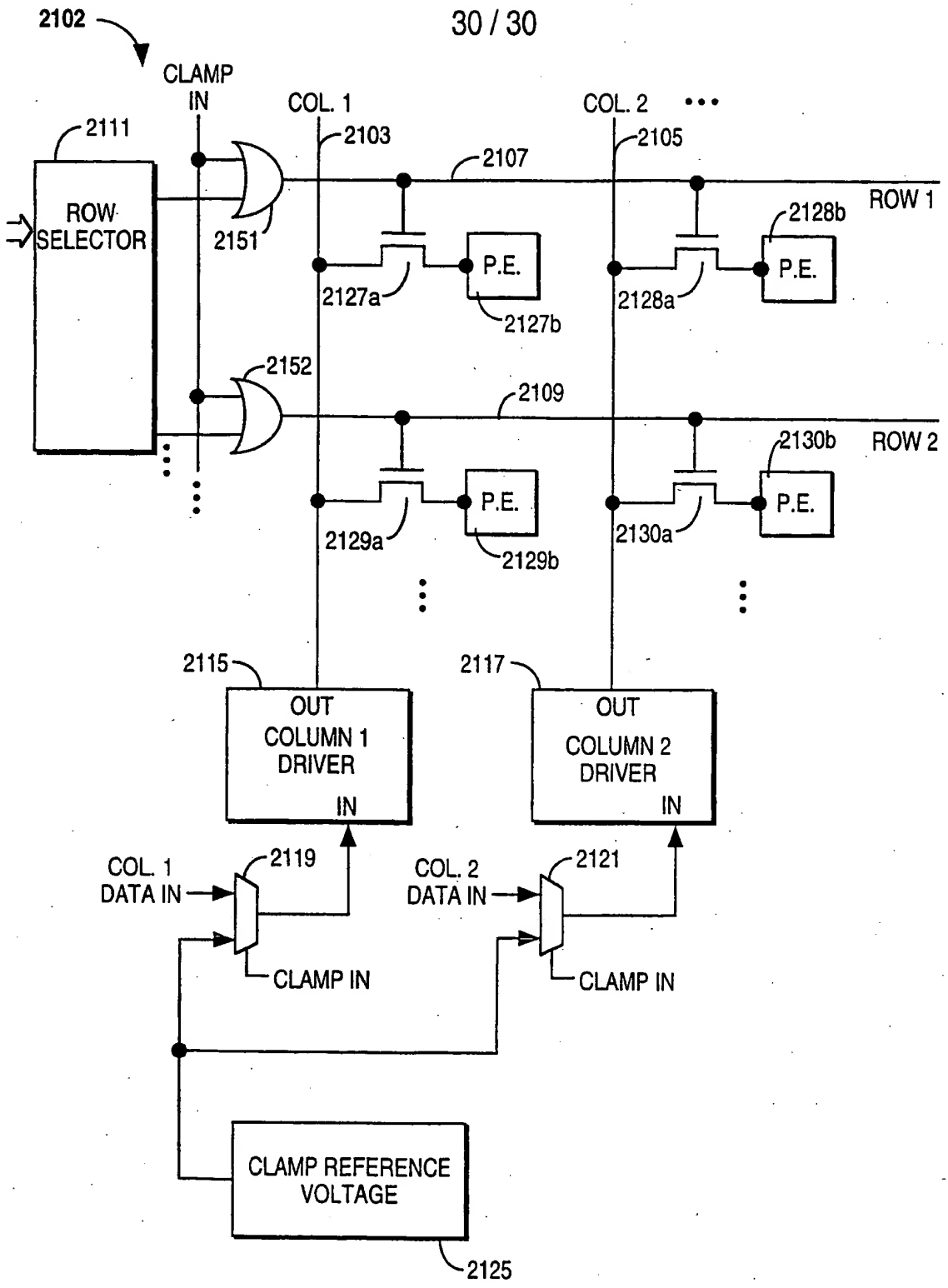

2102
CLAMP IN
COL. 1
COL. 2
2111
2103
2105
2107
ROW SELECTOR
2151
ROW 1
2128b
P.E.
2127a
2127b
2128a
2152
2109
2130b
ROW 2
2129a
2129b
2130a
2115
2117
OUT COLUMN 1 DRIVER IN
OUT COLUMN 2 DRIVER IN
COL. 1 DATA IN
2119
COL. 2 DATA IN
2121
CLAMP IN
CLAMP REFERENCE VOLTAGE
2125

FIG. 22

INTERNATIONAL SEARCH REPORT

In tional Application No
PCT/US 97/21919

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G09G3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 95 34986 A (PHILIPS ELECTRONICS NV ;PHILIPS NORDEN AB (SE)) 21 December 1995 see page 3, line 32 - page 4, line 32 see page 5, line 20 - page 6, line 23 see figures 1,5	1-7,9, 10,12-16
X Y	EP 0 660 297 A (SHARP KK) 28 June 1995 see page 14, line 29 - page 15, line 14 see page 16, line 42 - page 18, line 19 see figures 20-23 see figures 25,27,28	12-20 1-10
X	EP 0 632 426 A (SHARP KK) 4 January 1995 see page 14, line 49 - page 16, line 47 see page 18, line 36 - page 20, line 32 see figures 8-10,25-27 see figures 31-33	16-20

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
27 April 1998	07/05/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Amian, D

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 97/21919

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 95 01701 A (PHILIPS ELECTRONICS UK LTD ;PHILIPS ELECTRONICS NV (NL); PHILIPS N) 12 January 1995 see page 4, line 27 - page 5, line 29 see page 11, line 17 - page 13, line 15 see page 18, line 11 - page 19, line 10 see page 20, line 6 - line 29 see page 25, line 6 - page 27, line 1 see figure 2	1-10

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 97/21919

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9534986 A	21-12-95	EP 0715753 A	12-06-96
		JP 9501516 T	10-02-97
		US 5627560 A	06-05-97
EP 0660297 A	28-06-95	JP 7175034 A	14-07-95
		CN 1114426 A	03-01-96
		US 5640259 A	17-06-97
EP 0632426 A	04-01-95	JP 7120722 A	12-05-95
		US 5691783 A	25-11-97
WO 9501701 A	12-01-95	EP 0666009 A	09-08-95
		JP 8500915 T	30-01-96